Engineering Specification

PART NAME	PART NUMBER
EMC Design Guide for Printed Circuit Boards	ES-3U5T-1B257-AA

LET	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
FR	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
LET	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
FR	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
LET	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
FR	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57
LET	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
FR	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76
LET	A	A																	
FR	77	78																	

	LET	FR	REVISIONS	DR	CK	REFERENCE
			Released: ES-3U5T-1B257-AA			
			Initial Release			PREPARED/APPROVED BY
20021001			AE00-I-11448433-000			J. A. Tracz, 32-31919

CHECKED BY	DETAILED BY
CONCURRENCE/APPROVAL SIGNATURES	
Design Engineering Supervisor	T. Hermann
Design Engineering Management	C. De Biasi
Manufacturing Engrg.	
Quality Control	
Purchasing	
Supplier Quality Assistance	

FRAME 1 OF 78	A	

PD
May 1988

3947a1e

Initial Release Date: OCTOBER 01 2002

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

TABLE OF EQUATIONS

ACRONYMS AND ABREVIATIONS

AC	Alternating Current
AWG	American Wire Gauge
BCI	Bulk Cable Injection
BW	Bandwidth
CE	Conducted Emissions
CI	Conducted Immunity
CM	Common Mode
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CS	Conducted Susceptibility
dB	decibel
DC	Direct Current
DM	Differential Mode
EC	European Community
E/E	Electrical/Electronic
EMC	Electromagnetic Compatibility
EME	Electromagnetic Effect
EMI	Electromagnetic Interference
EPDS	Electrical Power Distribution System
ESC	Electronic Subsystem Component (Device Under Test)
ESD	Electro Static Discharge
EU	European Union
FCC	Federal Communication Commission
FET	Field Effect Transistor
FMC	Ford Motor Company
HSIC	High Speed Integrated Circuit
IC	Integrated Circuit
IEC	International Electrotechnical Commission
I/O	Input/Output
ISO	International Standards Organization
LSI	Large State Integration
MCU	Micro-Controller Unit
MOV	Metal-Oxide Varister
NB	Narrowband
PCB	Printed Circuit Board
PWB	Printed Wiring Board
PWM	Pulse Width Modulation
RE	Radiated Emissions
RF	Radio Frequency
RI	Radiated Immunity
RS	Radiated Susceptibility
SAE	Society of Automotive Engineers
TEM	Transverse Electromagnetic (Cell)

PART I: PREFACE

1. INTRODUCTION

Due to the tremendous increase in the use of electronic devices, ensuring Electromagnetic Compatibility (EMC) of a full system in its early design phase is becoming one of the major technical issues, especially for automotive manufacturers. Safe and reliable operation must be guaranteed and legal requirements have to be satisfied. From both car-makers and suppliers sides, the electromagnetic problems occur either when integrating electronic devices in their operating environment (cross-coupling, interference) or when dealing with the related EMC regulations (simulation of radiating phenomena due to Common-Mode currents induced on attached cables). As digital devices become smaller and perform at greater speeds, their emissions increase, making a thorough understanding of Electromagnetic Interference (EMI) essential for everyone in electrical engineering and design today.

This document contains design guidelines to aid in achieving EMC (Electromagnetic Compatibility) in automotive electrical/electronic components and systems. None of the material presented herein is new. On the contrary, it is based on well-established EMC measures and techniques, and on specific automotive EMC experience accumulated over the years within Ford Motor Company. The "EMC design guide for PCB" simply attempts to collect that wisdom together.

It should be pointed out that Parts 1 through 6 of this document are meant to be strictly informative. For example, the various design techniques presented in Section 5 are derived from a set of fundamental principles, and although the techniques aid each other in achieving electromagnetic compatibility, they don't guarantee it. Suppliers are ultimately responsible for assuring full Ford EMC compliance of their products.

Completion of Part 7 is mandatory.

The reader is encouraged to forward any comments, questions or suggestions regarding this document to the following e-mail address:

mailto:contact@fordemc.com

PART II: GENERAL EMC

2. EMC OVERVIEW

The application of electronic components and devices is increasing in all area of consumer products as well as within the industrial production environment. This provides an electromagnetic environment with an increasing overall noise floor due to digital control applications in virtually any niche of daily life and an ever increasing demand on mobile telecommunications facilities.

The noise margin – observations in the early 90's have revealed an increase of approximately 3 dB per year – poses an increasing threat onto the immunity margins of the electronic components. In contrast to the aggression, the immunity margin is falling due to the drastic increase in the complexity of the components, calling for a reduction in power consumption in order to control thermal effects for instance. The attempt of controlling costs also leads towards a trend of replacing solid metal housings with plastics or composites, which decrease shielding capabilities.

In summary, the trend in Electronics' applications, a raise of a harsh electromagnetic ambient has to be noticed with a loss of safety margins, making applications more susceptible to electromagnetic interference and calling for regulations to keep the problems arising under control.

2.1. The Elements

Electromagnetic radiation due to the operation of electrical or electronic devices may be grouped into two types:

- Intentional Emissions
- Unintentional Emissions

Examples of the first type are television and radio broadcasting systems, communication and radar systems, and transmitters for navigational purposes. However, even when performing properly such equipment may also generate undesired electromagnetic emissions of the second type. This might interfere with the system itself or the overall emissions might affect other sensitive equipment nearby. In order to control these kind of effects frequency management is necessary in the first place due to the fact that a certain part of the emission profile contains valuable information and is intended to be there.

Electronic components provide a frequency band and due to non-linearities in active devices unintentional harmonics may be created, and modulations might occur. In general, sources of coherent electromagnetic emission at a given frequency or within a specified frequency band are intentional transmitters, but both coherent as well as non-coherent emission bear the potential for electromagnetic interference problems. Electromagnetic emissions may thus be divided into:

- Radiation due to radio transmitters and similar nearby electrical or electronic equipment
- Transient environment caused by electrical switching operations, electrostatic discharge and lightning

2.2. The Environment

There are two fundamental classes of transfer types:

- Analogue
- Digital

The difference is not only due to the information coding but with regard to EMC the main difference is due to the quality and vulnerability.

Analogue circuitry reacts immediately on perturbations but the effects remain within relatively small limits, they might cause a rectification and possibly a drifting of the operation point. Typically, analogue circuitry recovers from the perturbation by turning back towards the regular operation. The operational safety margin corresponds to the signal to noise ratio.

In contrast to the above, digital circuits provide a 'large' safety margin because of the switching thresholds for the different states. Hence a digital application appears more robust than an analogue one. However, the move towards low voltage logic, 3V and even less, will reduce these margins. Another difference lies in the quality of failure which might be quite unpredictable for digital application – a bit might switch and cause a system to malfunction in the case of switching to a defined state or to hang because of turning into an undefined state.

Most problems associated with digital circuits are due to the high bandwidth inherited from the high-speed clocks and edge rates. Rise times in the realm of a few nanoseconds are equivalent with bandwidths well above 300 MHz range and the increase of the clock rates will drive this into the microwave range. In other words, higher bandwidths increase both emissions and the susceptibility of the circuitry.

This issue is fundamental to the functioning of the designed circuitry and comprises mainly the aspects of internal or intra-system EMC and Signal Integrity. Intra-system EMI includes problems due to mixed technologies, e.g. analogue and digital, or electromechanical and digital. In the former case, the noise created by the digital circuitry due to the impulsive nature of the power demands might cause some jamming of the analogue circuits. In the latter case, the noise due to motors and switching relays typically causes jamming of the digital circuits. In the case of high speed digital application the digital circuitry might also cause some malfunctions due to crosstalk between such high speed applications and reflections on the interconnects. A particular characteristic of analogue components is that they typically operate at low frequencies and low levels and in addition show very high input impedances.

2.3. Regulations and Standards

E/E devices on Ford products must comply with a variety of requirements mandated by:

- Federal Communications Commission (FCC) regulations
- Ford EMC specifications
- European Community (EC) EMC Directive

Within the United States, the **FCC** is responsible for radio spectrum allocations and assignments outside the federal government sector. FCC 15J is the FCC document that controls the interference potential of electronic computing devices. A computing device is defined as any electronic device or system that uses digital techniques. This encompasses any device that intentionally generates and utilizes frequencies in excess of 10 kHz. The FCC regulates transmitters and receivers under a different rule.

Vehicle radios and remote controlled transceivers must comply with FCC regulations. Most other E/E modules designed exclusively for a vehicle use, have Section 1 exemption from FCC regulations. However, Ford has a policy of voluntary compliance for all modules.

The FCC regulates the amount of radiated EMI from an E/E device. Table 2–1 compares the maximum radiated electric fields allowed by Ford and the FCC. The table shows the electric field strength in dBμV/m and μV/m. FCC Class B limits are for consumer-type computing devices.

Ford EMC requirement limits are derived from a variety of SAE, International Standards Organization (ISO), and EC standards. The latest version of the primary Ford component level EMC specification is available on line at www.fordemc.com.

By inspection of Table 2–1, it is evident that the Ford limits are much more stringent than those of FCC; especially when one considers that FCC limits are measured 3 meters away from the radiating device while Ford measurements are taken at 1 meter. The Ford limits are more restrictive for two primary reasons:

- Radiating devices on the vehicle are closer to radio transceivers on board the vehicle
- A vehicle contains many radiating devices

Table 2–1. FCC and Ford RE Limits

Ford RE limits (ES-XW7T-1A278-AB) (1 meter)		
Frequency (MHz)	µV/m	dBµV/m
0.15 – 25	31.6	30
25 – 200	3.2	10
200 – 1000	3.2 – 15.8	10 – 24
FCC Class B RE limits (3 meters)		
30 – 88	100	40
88 – 216	150	43.5
216 – 1000	200	46

Outside the United States, the European Community (**EC**) has recently passed a uniform EMC directive. Any electronic product and vehicle manufactured in the United States or elsewhere must fulfill the EC regulations before they can be marketed in Europe. The main EC EMC Directive for automotive is 95/54/EC (and UN-ECE R10.02).

2.4. Elements of EMI

Figure 2–1 shows the elements of an EMI situation. A generator is an E/E device that produces EMI. A receptor is an E/E device that receives or couples in EMI. A coupling path allows EMI from the generator to produce an undesired response in the receptor.

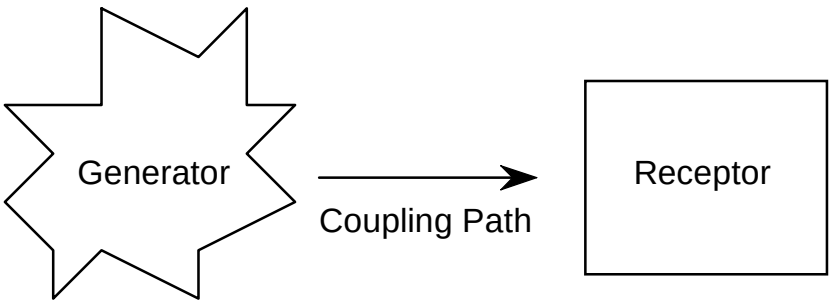


Figure 2–1. Elements of EMI

There are 3 ways in which to minimize the EMI:

- Reduce the noise from the generator
- Alter the coupling path
- Improve the immunity of the receptor

Reducing the noise from the generator may include reducing the generator circuit area, using a slower rise and fall time of a switching signal, using slower digital logic, reducing the circuit current, re-orienting the generator circuit on PCB, filtering, and/or shielding.

Often the designer must contend with the generator noise. This leaves either reducing the coupling path or hardening the receptor. Minimizing the coupling path may include moving the receptor away from the generator, re-orienting the receptor and/or generator on PCB, or shielding the receptor or generator.

Increasing the immunity of the receptor may include reducing the receptor circuit area, re-orienting the receptor circuit on PCB, using less susceptible electronic components, changing the impedance of the circuit, filtering, and/or shielding.

PART III: DESIGN APPROACH

3. OVERVIEW

Each unit of the overall system must be designed to meet the EMC Specified Limits. These EMC requirements can be divided into two primary categories: immunity (susceptibility) requirements and emission requirements.

3.1. Design Approach for Immunity (Susceptibility)

The different susceptibility requirements differ in threat energy and frequency content, although there is considerable overlap of these parameters among the test requirements. Of these requirements, the two susceptibility requirements that impact the design the most are the **Radiated Immunity** (**RI**) requirements, and the effects of **Electrostatic Discharge** (**ESD**) requirements.

3.1.1. Design Approach for Radiated Immunity

The Radiated Immunity threat is characterized by moderately high energy and very high frequency that can propagate in unexpected ways to circuit components, causing unexpected effects. The frequency range of radiated immunity can be found in the latest version of the component level spec at www.fordemc.com. Historic component level RI data shows that the band of frequencies most likely to cause radiated immunity-related problems for electronic controllers in an automotive environment is 10 MHz to ~ 900 MHz. The overall design approach for Radiated Immunity is to keep RI interference contamination out of the **ESC** (Electronic Subsystem Component) by removing it from signal and power lines entering the ESC (at ESC entry point).

3.1.2. Design Approach for ESD

The ESD threat is primarily characterized by short duration, high energy pulses that can damage I/O components or cause circuit upset. The frequency range of ESD is from DC to ~300 MHz (DC - 10MHz for lightning). The design approach for Radiated Immunity will also help prevent circuit upset caused by the high frequency components of ESD. However, ESD protection requires additional measures to prevent damage from the low frequency, high energy content of the induced ESD threats. Therefore, the overall design approach for ESD protection is to maintain high impedance, with respect to chassis ground, on signal and power lines to the ESC to minimize the effect of damaging ESD current and the corresponding energy from entering the ESC.

3.2. Design Approach for Controlling Radiated and Conducted Emissions

The purpose of emission requirements is to provide a level of assurance that the equipment will not produce electromagnetic emissions great enough to adversely affect the performance of other equipment in the vehicle (primarily communication, audio and electronic vehicle control systems). Fortunately, many of the design techniques used to

prevent Radiated Immunity and ESD interference energy from entering the ESC also prevent internally generated emissions from leaving the ESC. However, there are several additional design techniques used to minimize electromagnetic emissions from the ESC. The overall design approach for reducing emissions from the ESC is to prevent or minimize the generation of high frequency interference voltage and currents as close to the interference source as possible. The objective is to stop emissions at their source, before they can cross couple to other circuits and signal lines that cannot be easily filtered.

3.3. Ground System

A low inductance ground system is the most important element in designing a PCB for EMC. There are three types of ground structures on PCB:

- Minimal
- Ground Grid
- Ground Plane

The **minimal** ground structure connects the ground points on PCB with random, high inductance connections to other ground points. This is the least desirable method from an EMC standpoint.

Maximizing the ground area on a PCB minimizes the inductance of the ground system, which in turn minimizes radiated emissions. In addition, the maximized ground area provides shielding to improve radiated immunity of the PCB.

Figure 3–1 shows the ground grid structure. A **ground grid** provides many lower-inductance paths for current to return to its source.

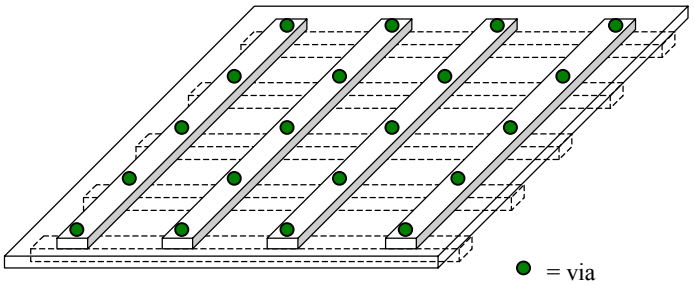


Figure 3–1. Ground Grid

Ground grid is achieved by connecting vertical and horizontal lines on opposite sides of PCB with vias. A **via** is a plated through hole that interconnects two or more PCB layers. Via connections also allow a signal track to 'jump over' a ground grid trace. All two layer PCBs should use a ground grid. In addition, multi-layer PCBs should use ground grids even if they employ one or more ground planes.

A **ground plane** is the lowest impedance conductor that serves as a current return and a signal reference. ***A ground plane is the ideal ground system***. It offers the lowest possible inductance for current to return to its source. A properly designed ground grid is the next best ground system.

Figure 3–2 compares the inductance of a ground grid and ground plane. The graph displays the inductance in nanohenries (nH) versus grid spacing in millimeters. To effectively lower the inductance of a ground grid the grid spacing must be less than 0.5 inches (~13 mm). Figure 3–2 shows that when the grid spacing equals 0.5 inches, the ground grid inductance has significantly decreased. Reducing the grid spacing further lowers the inductance.

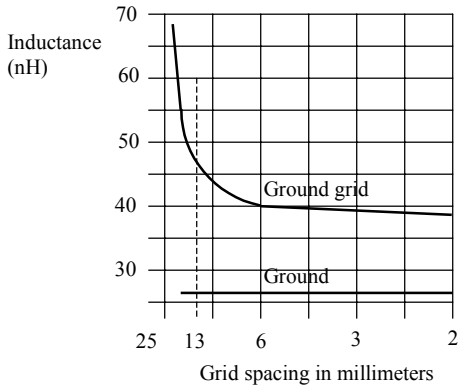


Figure 3–2. Inductance of Grounds

The inductance of a ground grid approaches but can never equal the inductance of a ground plane. They have equal inductances only when the grid spacing equals zero (when the ground grid becomes a ground plane).

Table 3–1 shows the impedance versus frequency for PCB tracks and ground planes. The ground plane is square and made of one-ounce copper (0.035 mm thick). The track is also 1 oz. copper with width of 1.0 mm and length 10.0 mm. These impedance calculations do not take into account the mutual inductance between a signal track and ground plane which would decrease the total impedance.

Table 3–1 indicates that the track has significantly more impedance than the ground plane due to a larger inductance. Ground inductance generates ground noise. This is the reason why ground planes generate less noise than a minimal ground system.

When high frequencies flow through the larger inductances of a minimal ground system they generate voltage drops within that system. Often this is the source of radiated emissions from a PCB. Ground noise voltages force EMI currents to flow out onto the wire harness that connects to the PCB. Moreover, the wires harness is usually much longer than the PCB, and thus it radiates more efficiently.

Table 3–1. Frequency and Impedance

Frequency	Ground plane impedance	Track impedance
100 Hz	574 μΩ	5.74 mΩ
1 kHz	574 μΩ	5.74 mΩ
10kHz	574 μΩ	5.76 mΩ
20 kHz	574 μΩ	5.81 mΩ
50 kHz	574 μΩ	6.14 mΩ
100 kHz	574 μΩ	7.21 mΩ
500 kHz	576 μΩ	22.5 mΩ
1 MHz	582 μΩ	44 mΩ
2 MHz	604 μΩ	87.5 mΩ
5 MHz	736 μΩ	218 mΩ
10 MHz	1.04 mΩ	437 mΩ
20 MHz	1.61 mΩ	874 mΩ
50 MHz	2.62 mΩ	2.18 Ω
100 MHz	3.69 mΩ	4.37 Ω
200 MHz	5.22 mΩ	8.74 Ω
500 MHz	8.26 mΩ	21.8 Ω
1 GHz	11.6 mΩ	43.7 Ω

Signal grounds usually fall into one of the three categories:

- Single-point ground
- Multi-point ground
- Hybrid ground

Single point grounds, (Figure 3–3), with regards to noise, are very undesirable because of the series connection of all the individual circuit grounds. At high-frequencies the inductances of the ground conductors increase the ground impedance. A single-point ground is preferable below 1 MHz. Between 1 and 10 MHz a single point-ground can usually be used, provided the length of the longest ground conductor is less than one-twentieth of a wave-length to prevent emissions and to maintain a low impedance.

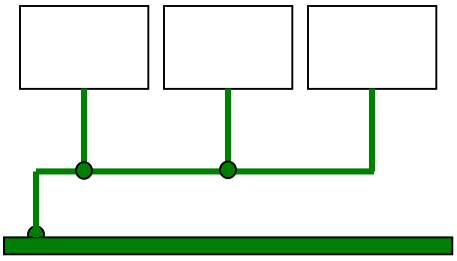


Figure 3–3. Single-Point Ground

Multi-point grounds, (Figure 3–4), have very low ground impedance and should be used at high frequencies and in digital circuitry. The low impedance is due primarily to the lower inductance of the ground plane. The connection between each circuit and the ground plane should be kept as short as possible to minimize their impedance. Multi-point grounds should be avoided at low frequencies since ground currents from all circuits flow through a common ground impedance – the ground plane.

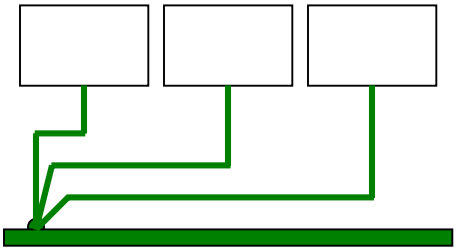


Figure 3–4. Multi-Point Ground

A hybrid ground, (Figure 3–5), is one in which the system grounding configuration appears differently at different frequencies – a single-point ground at low frequencies, and a multi-point ground at high frequencies. When different types of circuits (low-level analog, digital, noisy, etc.) are used in the same system or on the same PCB, then each must be grounded in a manner appropriate for that type of circuit. The different ground circuits should be tied together, usually at a single point.

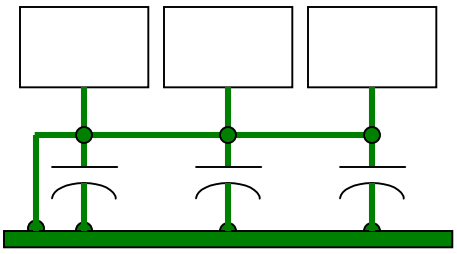


Figure 3–5. Hybrid Ground

3.4. Wavelength and Frequency

All electrical signals travel as waves with a finite velocity. Figure 3–6 shows the amplitude plot of a wave as a function of time. Its **wavelength** is the distance between any two equivalent points on the waveform.

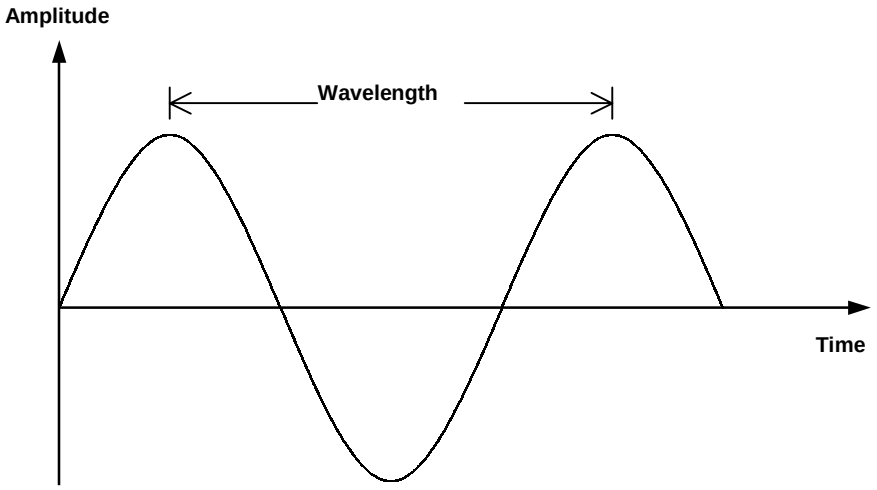


Figure 3–6. Wavelength of an Electrical Signal

The propagation medium determines the wave's velocity. In space a wave travels at the speed of light ***c*** ($c = 3 \times 10^8$ meters/second). However, the wave travels more slowly through wires or printed circuit board tracks (approx. 0.6 the speed of light).

Equation 3–1 relates wavelength (λ) to frequency in free space or in air. Table 3–2 shows that the wavelength and frequency are inversely proportional. Consequently, as the frequency increases, the wavelength will decrease.

$$\lambda = \frac{300}{f\ (MHz)} \quad \text{[meters]}$$

Equation 3–1. Wavelength

The atmosphere contains many electromagnetic fields generated by transmitters, which operate in a range from a few kilohertz to many gigahertz. Table 3–3 shows some of the frequency spectrum allocations in the United States (US), Europe (E), and Japan (J). All undesignated sources are in the United States.

Table 3–2. Wavelength as Function of Frequency

Frequency	λ
10 Hz	30,000 km
60 Hz	5,000 km
100 Hz	3,000 km
1 kHz	300 km
50 kHz	6 km
100 kHz	3 km
500 kHz	600 m
1 MHz	300 m
10 MHz	30 m
100 MHz	3 m
1 GHz	30 cm
10 GHz	3 cm

It is crucial that the E/E devices installed in a vehicle are immune to the fields produced by transmitters such as those listed in Table 3–3. In addition, the vehicle's E/E devices must not generate emissions that interfere with the intended receivers of these transmitters.

Table 3–3. Frequency Allocation and Usage Designation

Source	Frequency (MHz)	Typical radiated power (kW)
AM (E)	0.15 – 0.285	320
AM (E & J)	0.525 – 1.605	600 & 500
AM (US)	0.53 – 1.71	50
Amateur	1.8 – 29.7	0.16 (mobile)
Citizens band	26.9 – 27.4	0.004
Amateur	28 – 30	0.2 (mobile)
Land mobile	29 – 54	0.1
Amateur	50 – 54	0.2 (mobile)
TV low VHF	54 – 88	100
Land mobile (E)	65 – 85	0.1
FM (J)	76 – 90	44
FM (US & E)	88 – 108	105
Aircraft	108 – 136	1
Land mobile (E)	120 – 160	0.1
Land mobile	132 – 174	18 – 100
Land mobile (J)	142 – 170	
Amateur	144 – 148	0.2 (mobile)
TV high VHF	174 – 216	316
Land mobile	216 – 222	0.2
Amateur	222 – 225	0.1 (mobile)
Land mobile (J)	335 – 384	
Land mobile	406 – 512	0.1
Land mobile (J)	450 – 470	
Amateur	430 – 450	0.1 (mobile)
TV UHF	470 – 806	5000
Land mobile	806 – 947	0.035
Cellular (AMPS)	806 – 947	0.003
Amateur, LM, GPS	1200 – 1600	
Cellular (PCS)	1700 – 2000	0.003
Bluetooth	2300 - 2500	

3.5. Frequency Domain of Digital Signals

A typical square wave is shown in Figure 3–7.

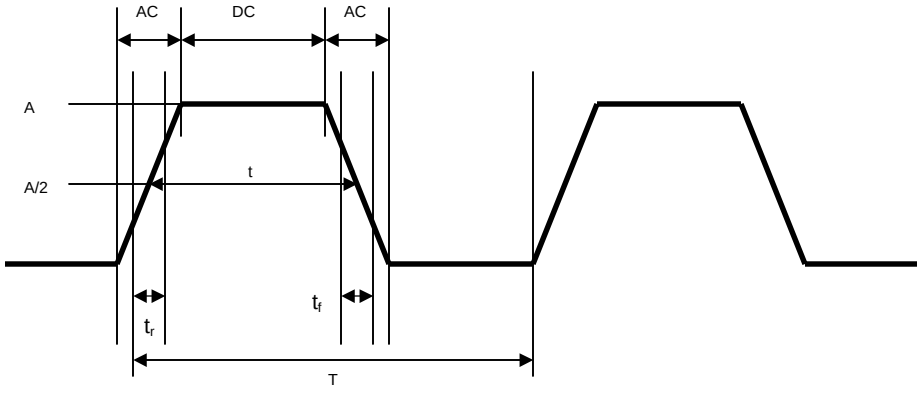


Figure 3–7. Elements of Digital Signal

A square wave has an AC component during the transition times and a DC component during the steady state. The AC current contains all of the frequency components of the square wave. In addition to the fundamental frequency, a digital signal also contains **harmonic frequencies** which are integer multiples of the fundamental frequency. For example, a digital signal with a fundamental frequency of 10 MHz has harmonic frequency components at 20, 30, 40, … MHz. Therefore, digital signal current flows at DC and at 10, 20, 30, 40, … MHz.

The signal spectrum is a plot of the fundamental and harmonic frequencies. Figure 3–8 shows the signal spectrum for a square wave in amplitude versus frequency graph.

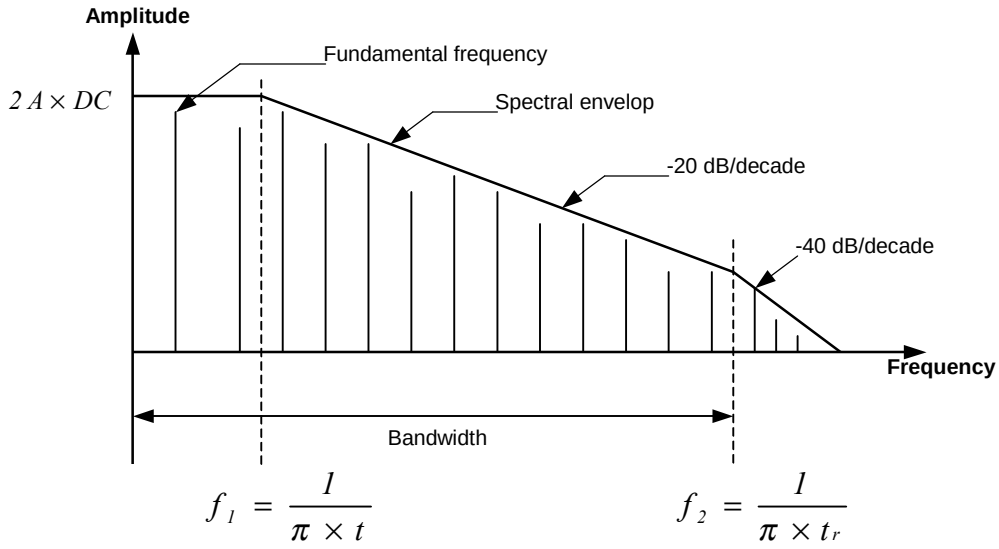


Figure 3–8. Digital Signal Spectrum

The **spectrum envelope** is a mathematical amplitude limitation of the spectral components of a digital signal. The maximum amplitude of the spectrum envelope equals *2A*×*DC*, where ***A*** is the peak amplitude of the square wave, and ***DC*** is a duty cycle (often denoted as ***δ***), then:

$$\delta = \frac{t}{T}$$

Equation 3–2. Duty Cycle

Where, ***t*** is the time that a square wave stays above one-half the maximum amplitude. The spectrum envelope falls off at 20 dB per decade at frequencies above $f_1 = 1/\pi t$.

The signal **rise time** (***t_r***) is the time that a digital signal takes to rise from 10% to 90% of its value (refer to Figure 3–7). Equation 3–1 states that the rise time determines the **bandwidth** (***BW***) of the signal. Use the signal **fall time** (***t_f***) if it is faster than the rise time, which it usually is. The spectrum envelope falls of at 40 dB per decade at frequencies above $f_2 = 1/\pi t_r$.

The magnitude (M) in dB at **> f_1** is computed as follows:

$$M(f_1 < f < f_2)_{dB} = M_1 = 20\log(2A\delta) - 20\log(\frac{f}{f_1})$$

$$M(f > f_2)_{dB} = M_{dB} = (f = f_2) - 40\log(\frac{f}{f_2})$$

$$BW = \frac{1}{\pi \times t_r}$$

Equation 3–3. Bandwidth

In Figure 3–8, the bandwidth contains 99% of the spectral energy of the signal.

The spectrum of the square wave in Figure 3–8 is also its Fourier series. Fourier theory states that a periodic signal can be expressed in terms of weighted sum of harmonically related sinusoids.

Equation 3–4 gives the amplitude for the fundamental and harmonic currents in the Fourier series of a square wave.

$$\left|I_n\right| = 2I_{max}\delta \frac{sin(n\pi\delta)}{n\pi\delta} \times \frac{sin\left(n\pi \frac{t_r}{T}\right)}{n\pi\left(\frac{t_r}{T}\right)} \quad \text{[Amperes]}$$

Equation 3–4. Current in Square Waves

Where, $1 \le n \le \infty$, I_{max} is the maximum current.

It is assumed that the rise and the fall times of a square wave are equal. A square wave with $\delta = 0.5$ has only odd numbered harmonic with the first current harmonic, $I_1 = 0.641 I_{max}$

3.6. Radiated Emissions Predictions

For intentional transmitters (e.g. broadcast towers), the electromagnetic field next to a transmitting antenna is very complex. This field is called the **near field**. However, the field becomes an uniform plane wave some distance from the antenna. This field is called the **far field**. The near to far field transition (equation below) occurs at about one-sixth of a wavelength from the transmitting antenna.

Near to far field transition: $\approx \frac{\lambda}{2\pi}$ [meters]

This next equation, Equation 3–5, shows how to calculate the far-field radiated emissions from any RF transmitter:

$$E = \frac{\sqrt{30 \times P_t}}{r} \quad \text{[Volts/meter]}$$

Equation 3–5. Far-Field Radiated Emissions

For example, the far field for a FM transmitter at 100 MHz occurs at about one-half meter. The transmitter electric field strength 100 meters (***r***) away from the transmitter (P_t=250 kW) equals 27.4 volts per meter.

For unintentional noise sources, E/E designers should consider circuit loops.
Equation 3–6 gives the maximum radiated emission in dBμV per meter from a small loop. **Differential mode (DM)** current, $\boldsymbol{I_n}$, is the normal signal or power current that flows in a loop.

$$E_{DM} = 20\log_{10}\left(2.63\times10^{-8}\ \frac{A\times f_n^2\times I_n}{r}\right) \quad [\text{dB}\mu\text{V/m}]$$

Equation 3–6. Radiated Emissions from a loop

Where, ***A*** is the area of a small loop
f_n is the spectral signal frequency
I_n is the spectral signal current
r is the distance from the small loop to the measurement antenna or the distance between a radiating generator loop and a receptor circuit.

Equation 3–7 predicts the maximum electric field in the far field from a small loop. It is accurate when the loop perimeter is less than one-quarter wavelength, and approximate for larger loops. In the near field multiply Equation 3–6 by Equation 3–7.

$$\vec{E}_{far\_field} = \sqrt{1+\left(\frac{\lambda}{2\pi\times r}\right)^2}$$

Equation 3–7. Far Field strength

Table 3–4 shows the radiated emissions at 1 meter from a PCB circuit with the following values:

Area = 5.0×10^{-4} meter^2 (5 cm×1 cm)
Fundamental frequency = 10 MHz
I_{max} = 10 mA
Rise time = fall time = 5 ns (typical high-speed CMOS)

Table 3–4. Sample RE Data

Frequency (MHz)	Current	Electric field (μV/m)	Electric field (dBμV/m)
10	6.34 mA	40.7	32.2
30	2.04 mA	45.5	33.2
50	1.15 mA	52.1	34.3
70	0.737 mA	47.5	33.5
90	0.494 mA	52.6	34.4
110	0.331 mA	52.7	34.4
130	0.214 mA	47.6	33.5
150	0.127 mA	37.6	31.5
170	63.7 μA	24.2	27.7
190	17.6 μA	8.4	18.4

Recall from Table 2–1 in Section 2.3 that the Ford RE limit from 1.8 MHz to 200 MHz is 10 dBμV per meter. Table 3–4 shows this PCB circuit would fail the RE limit set by ES-XW7T-1A278-AB spec at all of the spectral frequencies.

The predominant contribution to radiated emissions is due to the so-called **Common-Mode (CM)** current flowing in cables attached to an electronic device, and acting as efficient antennas in the frequency range which is considered (up to 2.5 GHz). The CM current is simply the net current in the cable. Ideally, this net current should vanish, because each current that enters the electronic device through the cable, also leaves it through the cable. Due to **parasitic effects**, this balance is disturbed and a CM current results. This CM current determines the amount of radiation because in the balanced case, the radiated field of each of the different wires in the cable almost cancel each other. Since only the net current in the cable is important, the cable may be considered as one single wire carrying this CM current. In automotive electronic devices several hundred different signals contribute to the overall CM current on attached cables. In order to estimate the contribution of the different nets, the basic CM current generation principle has to be understood and two basic mechanisms, i.e. current-driven and voltage-driven current excitation, need to be considered.

The **current-driven** mechanism is due to the partial inductance of the return currents in the ground plane, which produces a voltage drop across the ground plane, and injects the CM current into the attached cable.

The second mechanism is **voltage-driven**, because the signal voltage directly drives the CM current through the parasitic antenna capacitance.

Figure 3–9 shows the setup for measuring CM currents from an electronic device. The cable (wire harness) connects the electronic device to a load box that contains all of the input circuitry and loads the device drives. A two-meter (2 m) harness is the standard length used for measuring radiated emissions from an electronic device at Ford. The electronic device, harness, and load box are placed over a ground plane.

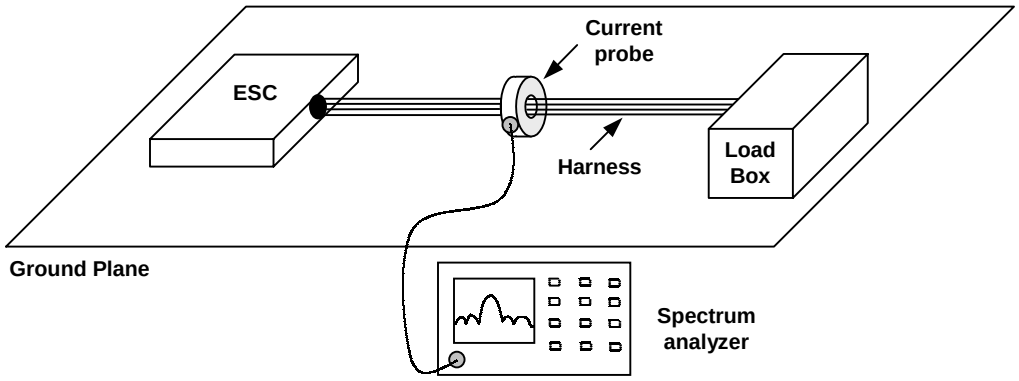


Figure 3–9. Setup for Measuring CM Currents

The RF current probe measures the net current that exits on the harness. Equation 3–8 gives the CM current calculation as:

$$I_{CM} = \frac{V_{SA}}{Z_t} \quad \text{[Amperes]}$$

Equation 3–8. Common Mode current

Where, V_{SA} is the voltage that the spectrum analyzer measures
Z_t is the probe transfer impedance in ohms

Equation 3–9 gives the electric field in dBμV per meter for a short wire (relative to wavelength) in free space due to the spectral amplitude of current I_n. Use this equation to estimate the electric field emissions due to CM current.

$$E_{CM} = 20 log_{10}\left(1.26 \frac{I_n L f_n}{r}\right) \quad \text{[dBμV/m]}$$

Equation 3–9. E-field strength due to CM current

Where, I_n is the spectral signal current
L is the length of the cable
f_n is the spectral signal frequency
r is the distance from the wire to a measuring antenna or the distance between a radiating generator wire and a receptor circuit.

Solving Equation 3–9 for the current gives Equation 3–10:

$$I_n = \frac{0.4 \times E}{f_n} \quad [\mu\text{Amperes}]$$

Equation 3–10. CM current

Where, $\boldsymbol{E}$ is in μV/m
$\boldsymbol{f_n}$ is in MHz

This equation includes the factors from ES-XW7T-1A278-AB specification, where the wire is two (2) meters long and the antenna distance from the wire harness is one (1) meter. It takes much less CM current than DM to result in the same Radiated Emissions.

Table 3–5 shows the maximum CM current that can flow on a single wire to just meet the Ford limit for radiated emissions. To find and measure the maximum CM current move the current probe along the harness length while monitoring the current with a spectrum analyzer.

Table 3–5. Ford RE Limit vs. Sample Data

Frequency (MHz)	Ford RE limit (dBμV/m)*	Ford RE limit (μV/m)	I (μA)
10	30	31.6	1.3
30	10	3.16	0.04
100	10	3.16	0.013
200	10	3.16	0.006

Note: Data obtained using Fischer F33-1 current probe.
* Limits per ES-XW7T-1A278-AB specification

3.7. Crosstalk

Vehicles contain many conductors such as wires, vehicle sheet metal, PCB tracks, and PCB ground planes. Wires can become a dominant factor since they may couple electromagnetic energy to other wires in the same bundle, and hence into an electronic device (module). **Crosstalk** is the coupling of signals between conductors. Crosstalk can occur through the following mechanisms:

- Common impedance coupling
- Capacitive coupling
- Inductive coupling

3.7.1. Common Impedance Coupling

Common Impedance Coupling exists when two or more circuits share a common conductor to source or sink current. The common impedance is a form of communication between the two circuits. Current passing through the common impedance develops a voltage, which appears directly in the receptor circuit. This shared impedance can occur in the automotive battery feed and ground distributions and shared signal voltage feed and signal returns. Common impedance coupling can cause many problems in PCBs and integrated circuits.

Figure 3–10 shows a common impedance in the positive and negative sides of a battery distribution circuit for two devices, A and B. Current flowing from circuit A raises the ground potential under circuit A and circuit B. Likewise, current flowing from circuit B has the same effect on circuit A. The voltage drop caused by current flow from either circuit changes the ground potential of the other (receptor) circuit. This is a form of communication between devices A and B, which may cause a problem, depending on the sensitivity of the other circuit. The same mechanism of common impedance occurs on the positive side of the battery.

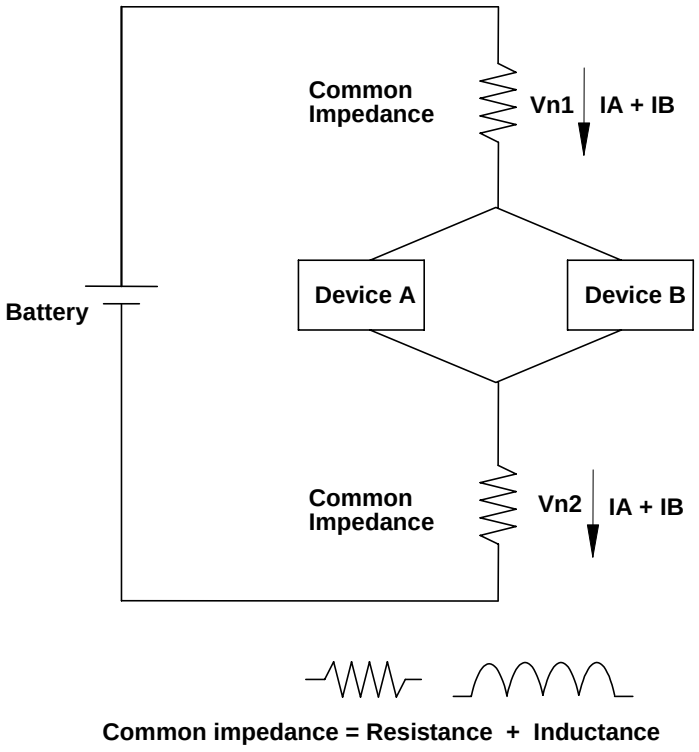


Figure 3–10. Elements of Common Impedance

3.7.2. Capacitive and inductive coupling

Figure 3–11 shows capacitive and inductive coupling between two circuits.

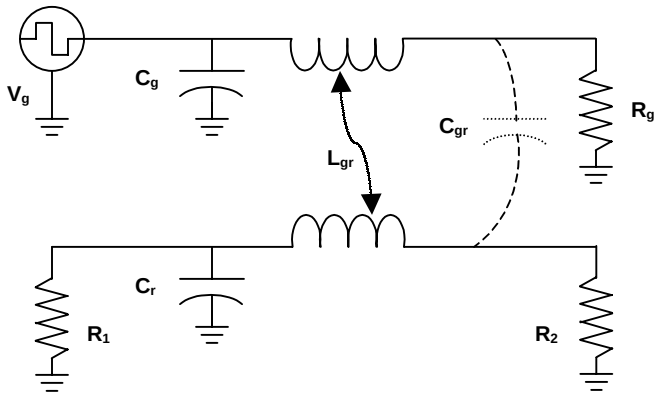


Figure 3–11. Inductive and Capacitive Coupling Between Two Circuits

Where, $\mathbf{V_g}$ is generator voltage
$\mathbf{C_g}$ is the generator capacitance
$\mathbf{R_g}$ is the generator circuit load
$\mathbf{R_1}$ and $\mathbf{R_2}$ are terminating resistances of the receptor circuit
$\mathbf{C_r}$ is the capacitance of the receptor circuit
$\mathbf{C_{gr}}$ is the mutual capacitance from the generator to the receptor circuit
$\mathbf{L_{gr}}$ is the mutual inductance from the generator to the receptor circuit

3.7.3. Capacitive coupling

A signal voltage creates an electric field from wires and PCB traces. Capacitive coupling results from the interaction of a time-varying electric field between a generator and receptor circuit. Figure 3–11 illustrates that capacitive coupling results from a mutual capacitance $\boldsymbol{C_{gr}}$. The mutual capacitance provides a path for EMI current to flow from the generator circuit to the receptor circuit.

Figure 3–12 shows the equivalent circuit for the capacitive coupling shown in Figure 3–11. $\boldsymbol{R_r}$ is the parallel equivalent circuit for $\boldsymbol{R_1}$ and $\boldsymbol{R_2}$. Whenever the generator signal changes, it induces a noise voltage in the receptor circuit. By inspecting Figure 3–12 one can see that capacitive coupling is essentially a differentiator circuit. The presence of $\boldsymbol{C_{gr}}$ differentiates the square wave to produce the receptor noise voltage.

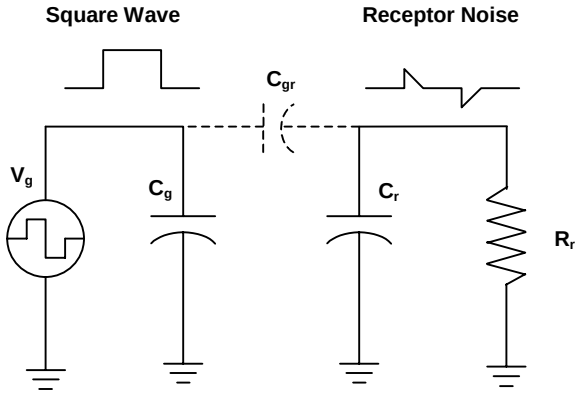


Figure 3–12. Capacitive Coupling

The amount of noise voltage that the generator circuit induces into the receptor circuit depends on the generator frequency and C_{gr}, which is largely a function of:

- Parallel length of the two circuits, and
- Separation between the two circuits

Equation 3–11 gives the mutual capacitance in picofarads per inch between two long conductors:

$$\frac{C}{l} = \frac{0.7\varepsilon_{r(eff)}}{ln\left[\frac{d}{r} + \sqrt{1 - \left(\frac{2r}{d}\right)^2}\right]} \quad \text{[pF/in]}$$

Equation 3–11. Mutual Capacitance in wires

Where, d is the distance between the center lines of the wires
r is the wire radius
ε_r is the permittivity of the wire insulation material.

The **effective permittivity**, $\varepsilon_{r(eff)}$ depends on the separation distance. It varies from $1<\varepsilon_{r(eff)}<3.2$

Equation 3–12 gives the capacitance in picofarads per inch between two wires over a ground plane.

$$\frac{C}{l} = \frac{0.7\varepsilon_{r(eff)} \ln\left[1+\left(\frac{2h}{d}\right)^2\right]}{\left[\ln\left(\frac{2h}{r}\right)\right]^2} \quad \text{[pF/in], for } \frac{2h}{r} >> 1$$

Equation 3–12. Mutual Capacitance

Where, ***d*** is the distance between the center lines of the wires
r is the wire radius
h is the distance between the center lines of the wires and the ground plane (hight)

Table 3–6 shows how mutual capacitance varies between two 18 gauge wires (radius = 0.024 inch) with and without a ground plane -- the ground plane returns the currents of both wires. The ground plane reduces the mutual capacitance between the wires by increasing the self-capacitance – the capacitance to its ground reference – on each wire. Butting wires show an increase in capacitance due to the dielectric constant of the wire insulation (PTFE with an E_r equal to 2.1).

Table 3–6. Mutual Capacitance in Two Wires

Separation Distance (inches)	No ground plane (pF)	Ground plane h = 02 in (pF)
Wires butting	18.77	6.28
0.1	6.16	3.01
0.2	3.99	1.71
0.5	2.77	0.53
1.0	2.25	0.16

Equation 3–13 gives the noise voltage, V_n due to capacitive coupling. R_f is the parallel equivalence of R_1 and R_2, which equals $2\pi \times f$, where f is the frequency or frequencies of V_g.

$$V_n = j\omega \times R_r C_{gr} V \qquad \text{whenever} \qquad R_r << \frac{1}{j\omega\left(C_{gr} + C_r\right)}$$

and

$$V_n = \left(\frac{C_{gr}}{C_{gr} + C_r}\right) V_g \qquad \text{whenever} \qquad R_r >> \frac{1}{j\omega\left(C_{gr} + C_r\right)}$$

Equation 3–13. Voltage Noise due to capacitive coupling

To reduce capacitive coupling:

- Decrease the generator frequency
- Decrease the parallel length between the circuits
- Increase the separation between the circuits
- Orient the receptor circuit to the generator circuit at 90˚
- Increase C_r
- Decrease R_r
- Shield the generator and/or the receptor circuit
- Place conductors over a ground plane

3.7.4. Inductive coupling

Inductive coupling results from the interaction of a time-varying magnetic field between a generator and receptor circuit. Inductive coupling can occur at low or high frequencies. Crosstalk from inductive coupling is more prevalent when high-level and fast-rising currents transients are conducted in a low-impedance circuits.

Signal current creates a magnetic field that surrounds the conductor. Figure 3–11 illustrates that conductive coupling results from a mutual inductance L_{gr}. The mutual inductance provides a path for magnetic flux to couple from the generator circuit to the receptor circuit.

Figure 3–13 shows that inductive coupling is essentially a simple magnetic transformer. The generator circuit is the primary and the receptor circuit is the secondary of the transformer. The figure also illustrates that when V_g is a sine wave then V_{noise} is a sine wave as well but with a reduced amplitude. When V_g is a square wave then V_{noise} shows noise spikes when the square wave changes.

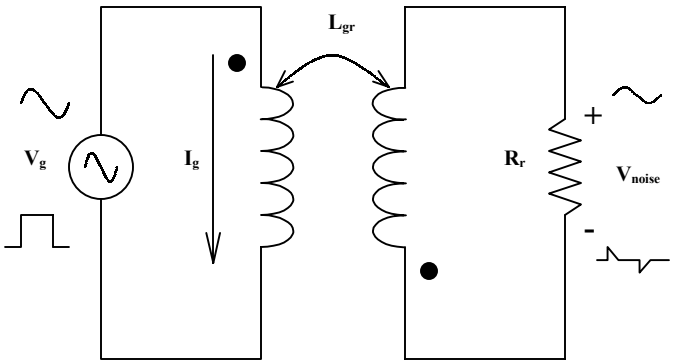


Figure 3–13. Inductive Coupling

The amount of noise voltage that the generator circuit induces into the receptor circuit depends on the generator frequency and L_{gr}, which is a function of:

- Receptor and generator area
- Parallel length of the two circuits
- Separation between the two circuits

Equation 3–14 gives the mutual inductance in microhenries per inch between two long circular conductors over a ground plane. The ground plane returns the currents of both circuits.

$$\frac{L_{gr}}{l} = 0.00254\, ln\left[1 + \left(\frac{2h}{d}\right)^2\right] \quad [\mu H/in]$$

Equation 3–14. Mutual Inductance

Where, h is the distance between the conductor centers and the ground plane
d is the distance between the center lines of the conductors

Figure 3–14 shows mutual inductance in microhenries per foot between two wires over a ground plane, versus the ratio of wire height to wire separation. The figure illustrates that mutual inductance increases as the areas of the generator and receptor circuits, increase.

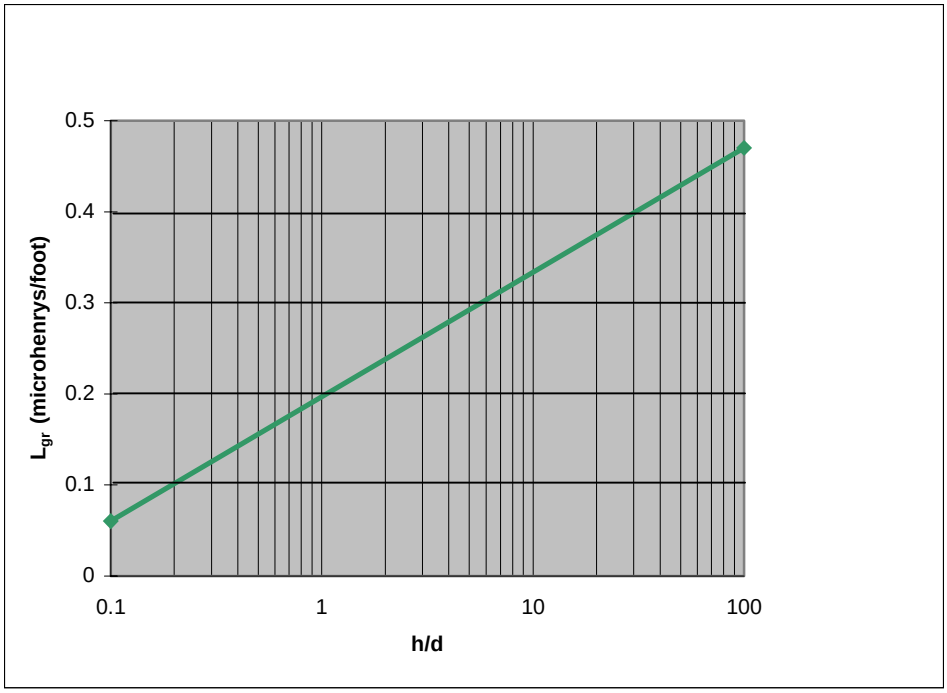


Figure 3–14. Mutual Inductance Between Two Wires

Equation 3–15 gives induced noise voltage from inductive coupling:

$$N_{noise} = L_{gr} \times \frac{di_g}{dt}$$

Equation 3–15. Noise voltage due to inductive coupling

Where, $\frac{di_g}{dt}$ is the rate of change of the generator current

Therefore, fast changing generator currents will induce larger noise voltages in receptor circuits.

Equation 3–16 also gives the noise voltage due to inductive coupling:

$$V_n = j\omega \times BA\cos\Theta$$

Equation 3–16. Noise voltage due to inductive coupling

Where, $\boldsymbol{B}$ is the magnetic flux density (weber/cm^2)
$\boldsymbol{A}$ is the receptor circuit area (cm^2)
$\boldsymbol{\Theta}$ is the angle between the generator and receptor circuit

3.8. Twisted Pair

A twisted pair of wires reduces inductive coupling by canceling induced magnetic field voltages. Figure 3–15 shows magnetic field (**B**) coupling into a circuit. V_s represents an input signal to an electronic device on a vehicle. R_{in} represents the input impedance of the module. The figure shows that the device input voltage, V_{in}, is the sum of V_s and the noise voltage V_n, which the magnetic field induces.

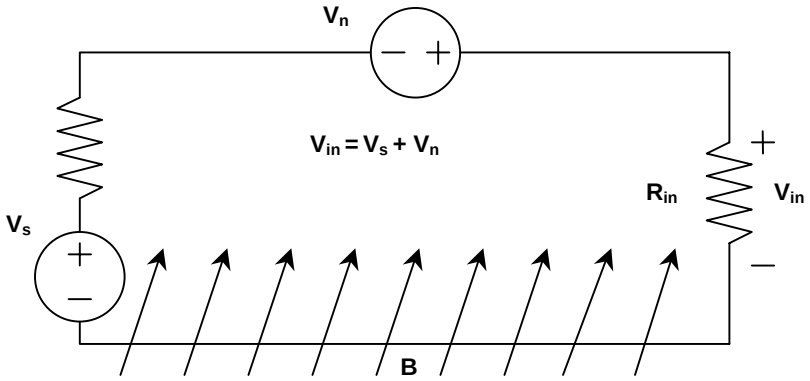


Figure 3–15. Magnetic Field Coupling into Circuit

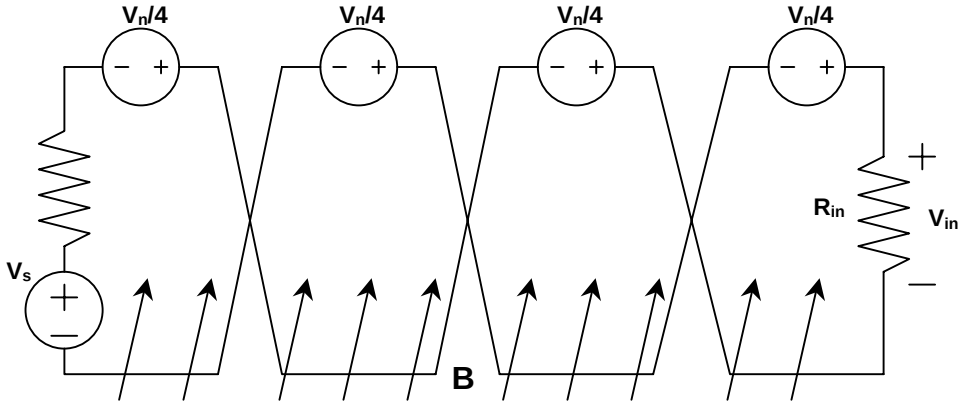


Figure 3–16. Magnetic Field Coupling into Twisted Wire Pair

Figure 3–16 shows the circuit in Figure 3–15 that uses a twisted pair. The twisting produces four equal loop areas with equal noise voltages. By summing all the voltages around the circuit the noise voltages cancel due to the twisting. This is why twisted pairs work best to reduce inductive coupling into a receptor circuit.

$$V_{in} = -\frac{V_n}{4} - \frac{V_n}{4} + V_s + \frac{V_n}{4} + \frac{V_n}{4} = V_s$$

Equation 3–17. Inductive Coupling in twisted-wire pair

To reduce inductive coupling:

- Reduce the receptor circuit area
- Increase the separation between the generator and receptor circuit
- Reduce the parallel length between the generator and receptor circuit
- Twist the receptor wires if the receptor current returns back through a wire
- Orient the receptor circuit to the generator circuit at 90˚
- Twist the generator wires if the generator current returns back through a wire
- Reduce the operating frequency of the generator circuit
- Reduce the rate of change of the generator current
- Reduce the generator circuit area
- Shield the receptor circuit with a shield grounded at both ends
- Use a shield of magnetic material
- Place the conductors over a ground plane. The ground plane must return the conductor currents

3.9. Shielding

EMI control must originate in the initial design of an E/E device. Some E/E devices require shielding to keep radiated energy away from module circuitry, or to keep EM energy from radiating from the module circuitry. Using a shield as a post-design fix to provide additional EMI protection adds cost and development time.

Shielding places a conductive partition between two regions in space. Shielding reflects and absorbs radiated EM energy, as shown in Figure 3–17. The noise source side of the shield reflects most of the incident energy, and the remaining energy enters the shield. As the field propagates through the shield, it absorbs some of the energy. When the field encounters the other surface of the shield some of it reflects back into the shield. The remaining electromagnetic energy enters the protected region.

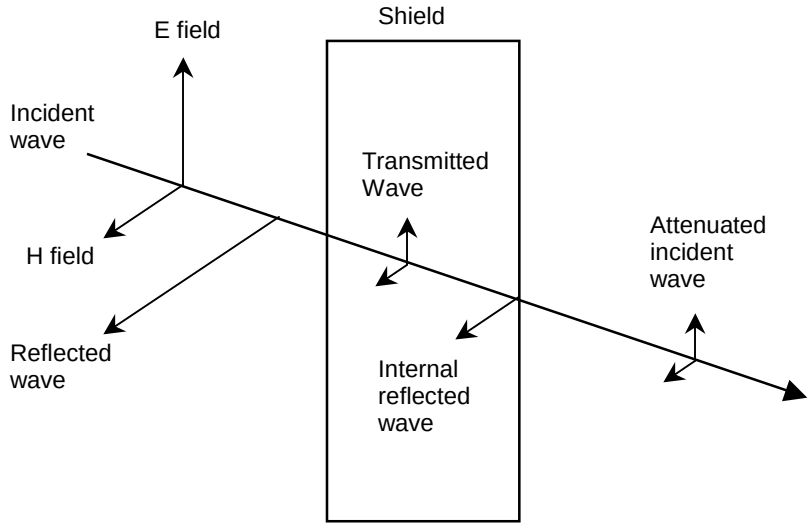


Figure 3–17. Effectiveness of Shielding

A shield presents two losses to electromagnetic energy:

- The **reflection loss (R)** is the air-to-shield and shield-to-air loss. Shield reflection varies with the type of field.
- The **absorption loss (A)** is the energy lost due to absorption as the field propagates through the shield. Shield absorption does not vary with the type of field. However, absorption loss varies with the type of shielding material.

Equation 3–18 shows that the **shielding effectiveness (SE)** is the sum of the reflection and absorption losses. The decibel is the unit of SE:

$$SE = R + A \quad [\text{dB}]$$

Equation 3–18. Shielding effectiveness

A SE of 40 dB indicates that the shield reflects and absorbs 99.99% of electromagnetic energy. Therefore, only 0.01% of EM energy penetrates the shielding system.

Magnetic material has a **relative permeability (μ_r)** greater than 1. Where μ_r is the ratio of the material's magnetic field conduction ability to air (μ_r varies with frequency). At ratios greater than 1, the magnetic field would rather conduct through the magnetic material than through the air. Table 3–7 shows the relative permeability of some common materials. The table also gives the relative conductivity of the material. The **relative conductivity (δ_r)** of the material is the ability to conduct current relative to copper. It is the inverse of **resistivity (ρ)**.

Absorption loss (A)

$$A = 3.34t\left(f \times \mu_r \times \delta_r\right)^{\frac{1}{2}} \quad [\text{dB}]$$

Equation 3–19. Absorption loss

Where, t is the thickness in inches

Shield absorption does not vary with the type of field. However, absorption loss varies with the type of shield material.

Reflection loss (R)

A shield can protect against the following:

- Electromagnetic (EM) field
- Electric (E) field
- Magnetic (H) field

Electromagnetic, electric, and magnetic fields require different shield design. An electromagnetic filed has both, an electric and magnetic fields oriented 90 degrees to each other. These fields travel together as the electromagnetic wave propagates through space. The electromagnetic field is usually referred to as a far field plane wave.

Any metallic shield will reflect electromagnetic and electric fields. Here, shielding is a function of:

- Frequency
- Shield thickness
- Shield's relative conductivity
- Shield's relative permeability
- Any openings (apertures) in the shield

In general, the field close to an E/E device is either primarily an electric or a magnetic field. For example, digital circuits on PCB generate a dominant electric field, whereas a motor generates a dominant magnetic field (at one-sixth of a wavelength distance from the generator circuit these separate fields do not dominate, and any radiated emissions become an electromagnetic wave).

In the near field, shielding is a function of the previously mentioned, and these additional factors:

- The impedance of the field generator
- The distance from the field generator

As previously mentioned, any metallic shield will reflect an electric field. However, only shields constructed from magnetic material are effective reflectors of magnetic field.

Table 3–7. Relative Permeability of Common Metals

Metal material	μ_r	d_r
Silver	1	1.05
Copper-annealed	1	1.0
Gold	1	0.70
Aluminum	1	0.61
Brass	1	0.26
Tin	1	0.15
Beryllium	1	0.28
Nickel	100	0.20
Stainless steel (430)	500	0.02
Iron	1000	0.17
Mu-metal (at 1 kHz)	20,000	0.03
Permalloy (at 1 kHz)	80,000	0.03

3.10. Resistance

Table 3–8 shows some wire characteristics (AWG is the American Wire Gauge).

Table 3–8. Resistance in Wires

AWG	Number of strands	Strand diameter (inches)	Cable diameter (inches)	MΩ per foot @ 20˚C
1	19	0.0664	0.332	0.1288
2	7	0.0974	0.292	0.1644
4	7	0.0772	0.232	0.2582
6	7	0.0612	0.184	0.4105
8	7	0.0486	0.147	0.6528
10	7	0.0385	0.116	1.028
12	7	0.0305	0.096	1.650
14	7	0.0242	0.073	2.624
16	7	0.0192	0.060	4.172
18	7	0.0152	0.048	6.636
20	7	0.0121	0.035	10.54
22	7	0.010	0.030	14.74

Equation 3–20 gives the resistance (***R***) of a solid copper slab:

$$R = \frac{1.724 \times 10^{-6} \times l}{wt} \quad [\Omega]$$

Equation 3–20. Resistance in Copper

Where, 1.724×10^{-6} Ω-cm equals the resistivity (ρ) of copper
t is the thickness in cm
w is the width in cm
l is the length of the slab in cm

Table 3–9 shows the resistance of grounding straps in milliohms per foot. The strap size gives the cross-sectional dimensions.

Table 3–9. Resistance in Grounding Straps

Strap size (cm)	Resistance mΩ/foot		
	Copper	Steel	Aluminum
0.05x0.5	2.11	11.85	3.27
0.05x1.0	1.06	5.93	1.64
0.05x2.0	0.53	2.96	0.82
0.1x0.5	1.06	5.93	1.63
0.1x1.0	0.53	2.96	0.82
0.1x2.0	0.26	1.49	0.41

3.11. Inductance

The inductance ***L*** [self inductance] of a circuit or device depends on geometry and the magnetic properties of the medium in and around the circuit or device. Larger circuits have more inductance. Devices such as solenoids that use a core of magnetic material have more inductance.

Inductive reactance is an inductor's resistance to a change in circuit current. Equation 3–21 gives the inductive reactance (impedance) versus frequency of an inductor:

$$Z_L = 2\pi \times frequency \times L \quad [\Omega]$$

Equation 3–21. Inductive Reactance

Where, ***L*** is the inductance of the conductor

Equation 3–22 gives the inductance of a rectangular conductor or ground strap:

$$L = 0.002l\left[2.303\log\left(\frac{2l}{w+t}\right) + 0.2235\left(\frac{w+t}{l}\right) + 0.5\right] \quad [\mu H]$$

Equation 3–22. Inductance in rectangular conductor

Where, ***l*** is the strap length in cm
w is the strap width in cm
t is the strap thickness in cm

Table 3–10 shows the inductive reactance for three ground strap widths. Each strap has a length of one foot (30.48 cm) and thickness of 0.05 cm. Note that doubling the strap

width does not reduce the impedance by one-half due to the logarithmic dependency of inductance in Equation 3–22.

Table 3–10. Inductive Reactance vs. Frequency

Frequency	Inductive Reactance Ω/foot		
	w = 0.5 cm	w = 1.0 cm	w = 2.0 cm
100 Hz	200x10-6	175x10-6	150x10-6
1 kHz	2.00x10-3	1.75x10-3	1.50x10-3
10 kHz	20.0x10-3	17.5x10-3	15.0x10-3
100 kHz	200.0x10-3	175x10-3	150x10-3
1 MHz	1.997	1.750	1.497
100 MHz	199.7	175.0	149.7
500 MHz	998.3	875.2	748.4
1 GHz	1,996.7	1,750.4	1,496.9

Figure 3–18 shows two wires where one wire carries signal or power current and the other wire carries the signal or power return current. Both wires have the same radius, ***r***.

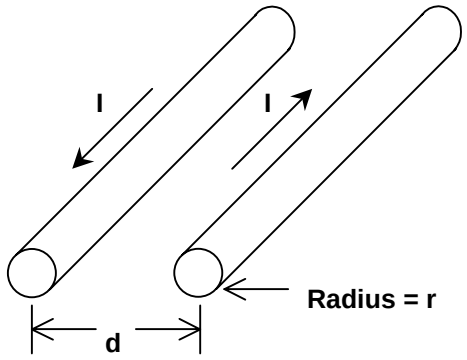


Figure 3–18. Inductance in Parallel Wires

Equation 3–23 gives the self-inductance in micro henrys per foot for two circular conductors of equal radii:

$$\frac{L}{l} = 0.12\,ln\left(\frac{d}{r}\right) \quad [\mu H/foot]$$

Equation 3–23. Inductance in parallel wires

Where, ***d*** is the distance between the center lines of the two conductors in inches
r is the wire radii in inches

Table 3–11 below, shows the impedance of various solid copper wire pairs versus frequency. Each wire has a length of one (1) foot and wire separation of one (1) inch. Note: wires with smaller diameters will have higher inductances.

Table 3–11. Impedance in Solid Copper Wires

Frequency	Inductive Reactance Ω/foot		
	4 AWG	16 AWG	22 AWG
100 Hz	172x10-6	277x10-6	329x10-6
1 kHz	1.72x10-3	2.77x10-3	3.29x10-3
10 kHz	17.2x10-3	27.7x10-3	32.9x10-3
100 kHz	172x10-3	277x10-3	329x10-3
1 MHz	1.72	2.77	3.29
100 MHz	172	276.9	329.3
500 MHz	860	1.38x10+3	1.65x10+3
1 GHz	1.72x10+3	2.77x10+3	3.29x10+3

Figure 3–19 shows a circular conductor of radius, ***r***, located at height, ***h***, over a ground plane. The ground plane returns the current that flows through the circular conductor.

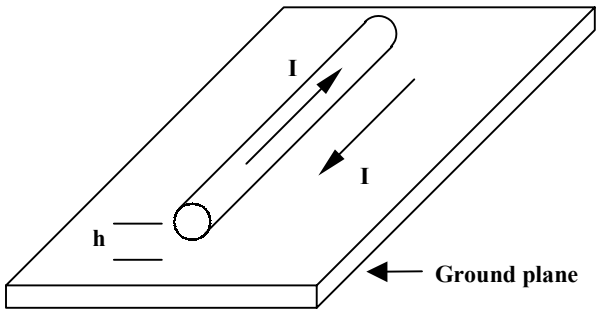


Figure 3–19. Inductance in Wires over Ground Plane

Equation 3–24 gives the self-inductance in micro henrys per foot for a circular wire over a ground plane, with ground plane returning the current. Note that the inductance is about one-half the inductance in Equation 3–23.

$$\frac{L}{l} = 0.06\, ln\left(\frac{2h}{r}\right) \quad [\mu H/foot]$$

Equation 3–24. Self-Inductance

Figure 3–20 shows the self-inductance, ***L(d)*** in micro henrys per foot of an 18 gauge solid-copper wire pair versus the ratio of the separation distance ***(d)*** to the wire radius ***(r)***. The wire separation varies from 0.1 to 10 inches and wire radius is 0.020 inches.

Figure 3–20 also shows the inductance, ***L(h)*** in micro Henrys per foot of an 18 gauge solid-copper wire over a ground plane versus the ratio of the wire height ***(h)*** to the wire radius ***(r)***. The wire height varies from 0.1 to 10 inches. Note the significant difference when a ground plane returns the current instead of a wire. The ground plane provides more mutual inductance to the wire to reduce the overall inductance circuit.

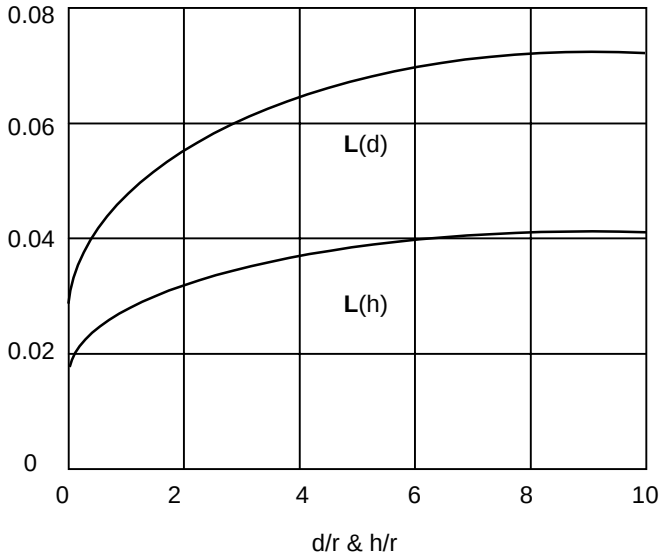


Figure 3–20. Inductance of Ground Plane vs. Wire Inductance

Table 3–12 also compares the self-inductances of the wires in Figure 3–20.

Table 3–12. Self-Inductance in Wires

Wire height (h) or wire separation (d) (inches)	L(h) Wire over ground plane μH/foot	L(d) Wire pair μH/foot
0.1	0.132	0.168
0.2	0.168	0.252
0.5	0.228	0.360
1	0.264	0.444
2	0.312	0.528
5	0.360	0.636
10	0.408	0.720

Equation 3–25 gives the inductance of an air-core inductor as:

$$L = \frac{r^2 \times N^2}{9r + 10l} \quad [\mu H]$$

Equation 3–25. Inductance in air-core inductors

Where, ***r*** is the core radius in inches
l is the core length in inches
N is the number of turns

Equation 3–26 gives the inductance of a toroid as:

$$L = 0.00508 N^2 \times b \times \mu_r \times ln\left(\frac{d_2}{d_1}\right) \quad [\mu H]$$

Equation 3–26. Inductance in toroids

Where, ***N*** is the number of turns
b is the core length in inches
d_1 is the inside diameter in inches
d_2 is the outside diameter in inches
μ_r is the permeability of the toroid material

PART IV: EMISSIONS FROM INTEGRATED CIRCUITS

4. SCOPE

With today's advancements in semiconductor technology and push towards faster MCUs and peripherals, the main concern is the amount of emissions generated by the microcontroller. At present, no single specification on the pass or fail criteria for integrated circuits exists, and limits in general depend upon the application, functional requirements, and local or mandated emission requirements.

In order to promote international co-operation concerning standardization in the E/E fields several procedures have been developed to facilitate verification of the electromagnetic behavior of integrated circuits. These test methods guarantee a high degree of repeatability and correlation of RE measurements. Ford recommends that integrated circuits, prior to ESC installation, be subjected to emissions profiling in order to quantify their EMI contribution to the overall system performance.

Rather than imposing a single limit on all integrated circuits, they ought to be classified according to their radiated emissions levels.

4.1. Applicable Documents

IEC Documents:

IEC-61967* "Integrated Circuits, Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz", IEC SC47A/WG9, 2001 or later edition

SAE Documents:

SAE-J1752/3** "Electromagnetic Compatibility Measurement Procedures for Integrated Circuits - Integrated Circuit Radiated Emissions Measurement Procedure 150 kHz to 1000 MHz, TEM Cell", SAE 1999 or later edition

Ford Documents:

XW7T-1A278-AB "Electronic Component EMC Requirements and Test Procedures", FMC 1999 or later edition

* IEC-61967, as part of International Standard IEC SC47A/WG9, is a project number for emissions test methods. This specification recommends test procedures to use and provides reference levels required in order to comply with automotive requirements

** SAE-J1752/3 procedure - for further details refer to this Society of Automotive Engineers manual, 1999 or later edition

4.2. EMC Test Recommendations

It is recommended that all applicable integrated circuits be subjected to radiated emissions testing according to procedures specified in International Standard IEC-61967* - "Integrated Circuits, Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz". The suppliers are encouraged to obtain test reports from IC manufacturers following the testing to establish a quantitative measure of RF emissions from ICs. The test reports should contain all salient information and parameters of the tests and test results. The reports should include test data, test set up description, photograph or sketch of the set up, software operating modes, and a summary of test results.

The recommended frequency range is 150 kHz – 1 GHz, but this may be extended if the specific procedure is usable over an extended frequency range.

4.3. Test Procedure Applicability

The following criteria may be used to determine if a part is a candidate for RE testing:

- Digital technology, LSI, products with oscillators or any technology which has the potential of producing radiated emissions capable of interfering with communication receiver devices. Examples include microprocessors, high speed digital ICs, FETs incorporating charge pumps, devices with watchdogs, switch mode regulator control and driver IC's
- For all new, re-qualified or existing IC's that have undergone revisions from previous versions

Examples of factors that would be expected to affect emissions are changes in the components:

- Clock drive (internal or external)
- I/O drive
- Manufacturing process or material composition that reduces rise/fall time
- Minimum feature size (die shrink)
- Package or pinout configuration
- Lead-frame material

4.4. IC Emissions Reference Levels

The IC emissions acceptance levels proposed by Ford differ from those proposed by SAE J1752/3** document, and are shown in Figure 4–1. These reference levels apply to measurements over the frequency range of 150 KHz to 1000 MHz in units of dBµV.

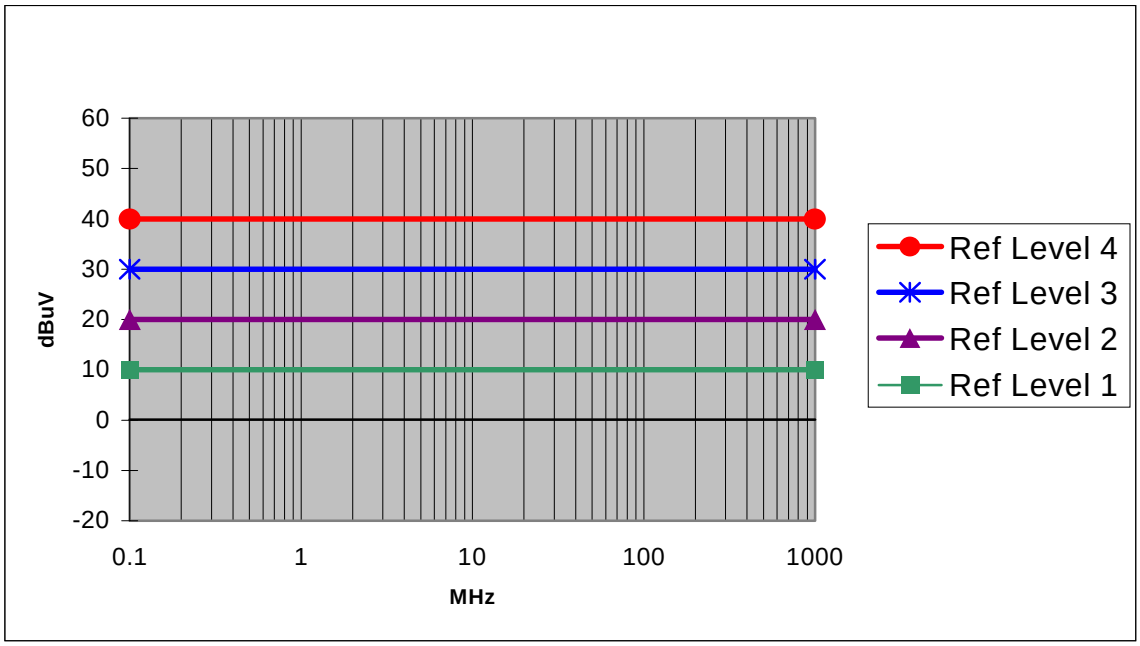


Figure 4–1. IC Radiated Emissions Acceptance Levels

Note: Limits for the TEM Cell are derived from the Magnetic Dipole Moment Reference Levels in SAE J1752/2 using the equation in J1752/3 Appendix D.

The following rating system was developed to help classify IC emissions:

Table 4–1. Rating Levels for IC's

Classification	Description
1	**RE** ≤ Reference Level 1
2	Reference Level 1 ≤ **RE** ≤ Reference Level 2
3	Reference Level 2 ≤ **RE** ≤ Reference Level 3
4	Reference level 3 ≤ **RE** ≤ Reference Level 4
NR – Not Recommended	**RE** ≥ Reference Level 4

4.4.1. Level 1

No EMC RE risk. Full EMC RE compliance may be achieved with minimum effort. Greatest flexibility in EMC design application. Potential cost reduction opportunity through reduction of:

- Number of components on PCB
- Material cost (single-sided PCB opportunity)
- PCB design iterations
- Testing cycles
- PCB assembly time

4.4.2. Level 2

Minor EMC RE risk. Less flexibility in EMC design than Level 1 but full compliance may still be achieved with little effort. Additional components and/or stricter adherence to industry's fundamental EMC design practices may be required.

4.4.3. Level 3

Moderate EMC RE risk. Close follow up of EMC fundamental design principles is strongly recommended. Additional preventive measures may be required, and may include the introduction of T-filters, Pi-filters, ferrites, inductors, etc. Extra PCB layers, components, and/or component shielding may also be necessary.

4.4.4. Level 4

High EMC RE risk. Strict adherence to EMC fundamental design principles is strongly recommended. Additional preventive measures, such as PCB shielding (metal housing), harness and/or component shielding, extra layers, T-filters, Pi-filters, ferrites, chokes, etc., may also be required at a substantial additional expense. Supplier(s) choosing Level 4 IC(s) should keep in mind that in order to implement and validate these additional preventive techniques an extra design time and/or test time may be necessary.

4.4.5. Level NR

IC(s) classified as category NR may not be able, even with extra preventive measures, to comply with Ford RE requirements and therefore should not be considered. ESC(s) with NR category parts found to exceed Ford RE requirements may be denied EMC approval.

4.5. Data Submission

It is recommended that suppliers request from IC manufacturers emissions plots (both orientations) along with setup information (ref. SAE-J1752/3**, figure 4) for all applicable integrated circuits prior to PCB layout. Such data should be available for review by Ford EMC personnel upon request.

4.6. Radiated and Conducted Immunity

If the supplier is aware of any radiated or conducted immunity concerns which have the potential of jeopardizing product robustness or timely delivery, Ford EMC representative should be notified immediately.

PART V: EMC DESIGN GUIDELINES FOR PCB

5. GENERAL

Electromagnetic compatibility MUST be considered early in the design stage of any E/E device. If it is ignored early in the design cycle, as problems are encountered during testing or in the field, fixes become very expensive – primarily because the design is less flexible.

A noise problem on a printed circuit board can be solved at the layout stage for a relatively small cost. However, if it is dealt with after the design has been completed the cost can increase 10 or even 100 fold. Figure 5–1 illustrates that EMC achieved at the design stage is a one-time cost, while EMI problems and fixes in the field can cost an enormous amount of time and money if engineering changes are necessary.

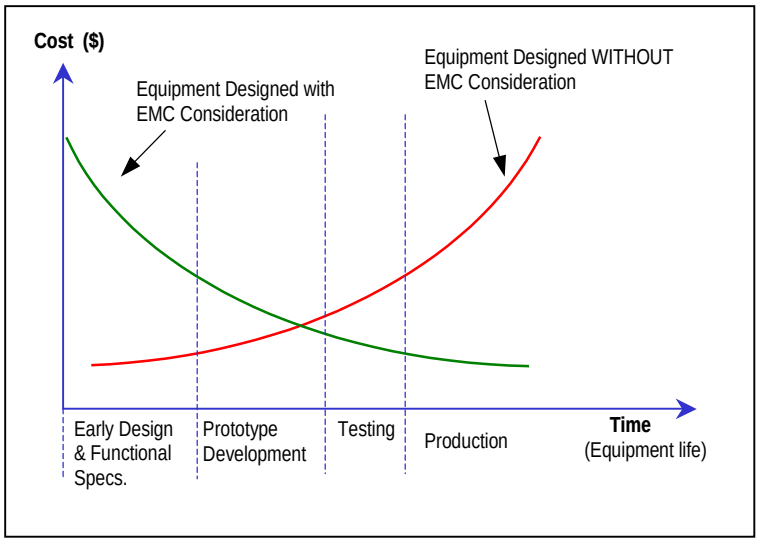


Figure 5–1. Relative Costs of EMC vs. NO EMC Design Strategy

Attention to good practices in circuit (hardware) design can provide inherent electromagnetic compatibility. Examples of such practices are decoupling power and I/O lines to ground, providing selectivity and voltage limiting, maintaining linearity, limiting signal bandwidth to only that needed by the circuit, using negative feedback, wave shaping, signal interlocks, synchronization, refresh cycling, and fault tolerant software.

5.1. Board Structure/Ground Systems

1. When creating a schematic each component should have an appropriate reference designator identifying it as a member of a specific functional group. This will assure correct placement of components on PCB during layout.

   A recommended arrangement of functional groups on PCB is shown in Figure 5–2. All components should be placed with an appropriate functional group and their tracks routed within their designated PCB area.

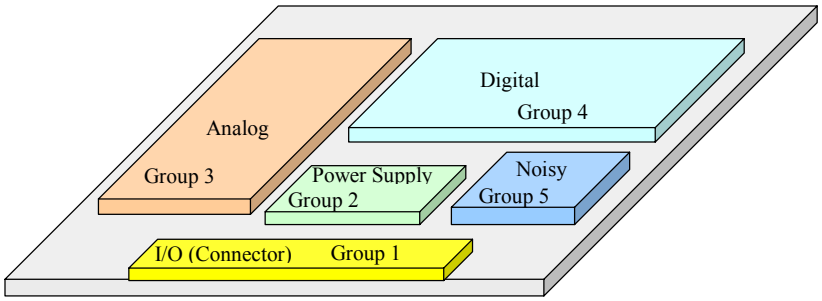


Figure 5–2. Arrangement of Functional Groups on PCB

2. Place ground plane(s) under all components and all their associated tracks - a continuous ground plane with no avoidance in IC package or I/O connector area is recommended. (Figure 5–3).

3. Maximize copper areas to provide low impedance for power supply decoupling - careful arrangement of components and connections (traces) may allow large areas of PCB to be filled with ground. Figure 5–3.

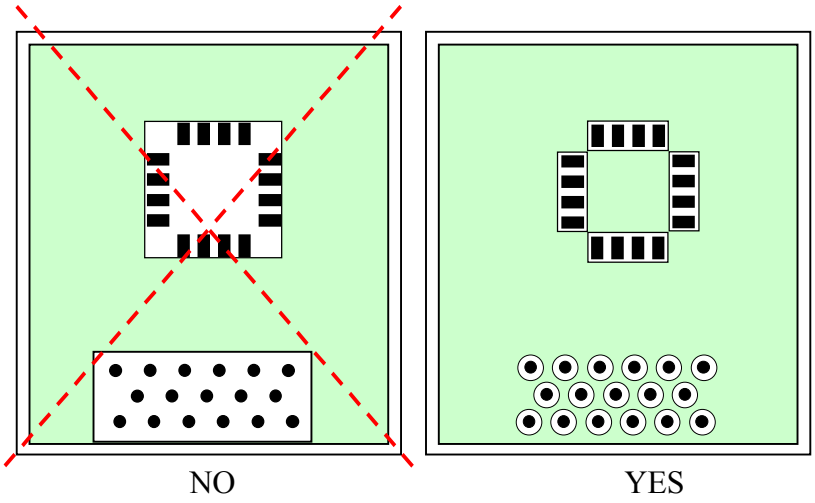


Figure 5–3. Maximizing Ground on PCB

4. All two-layer PCBs, where ground plane is not feasible, should utilize a ground grid system.

   The top and bottom side of PCB should look like a ground plane with horizontal ground tracks on one side, and vertical ground tracks on the other side. Ground grid traces should be as wide as possible and be placed apart as close as possible. A ground grid is achieved by connecting vertical and horizontal lines on opposite sides of PCB with vias. A via is a plated through hole that interconnects two or more PCB layers. In addition, multi-layer PCBs should use ground grids even if they employ one or more ground planes. A properly designed ground grid is the next best ground system (Figure 5–4)

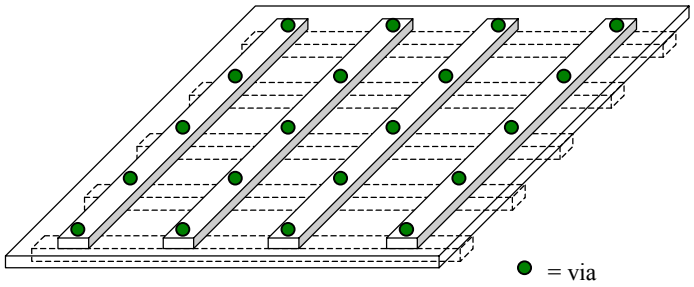


Figure 5–4. Ground Grid Technique

5. Install ground vias around the perimeter of the PCB every 0.5 inches or less as shown in Figure 5–5. Connect these vias together with 15 mil (0.4 mm) minimum trace thickness on all layers.

   This should help to contain frequencies up to 5 GHz on the PCB board by forming a "Faraday's cage". Routing of traces outside the ground vias should not be permitted except for connections with the 'outside world'.

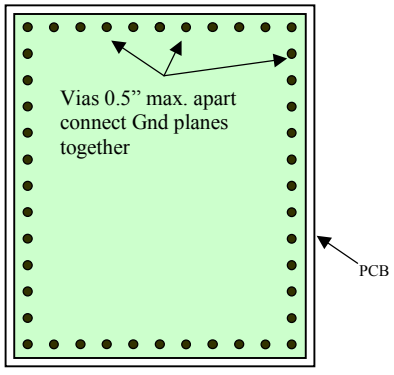


Figure 5–5. Creating 'Faraday's Cage'

6. For multi-layer boards the recommended layer stack-up is shown in Figure 5–6.

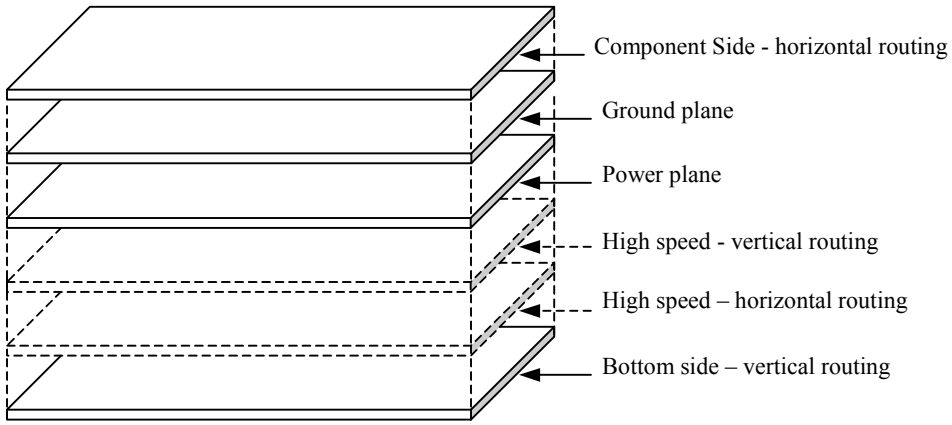


Figure 5–6. Layer Stack-up

7. On boards without a ground plane, i.e. two-sided boards, power and ground traces should be routed adjacent to or on top of one another on different layers to reduce loop area (Figure 5–11).

8. A solid ground 'island' should exist underneath all High Speed Integrated Circuits (HSICs) on surface layers. Figure 5–7.

9. Whenever possible, place a ground via next to all IC's ground pins as shown in Figure 5–7. Frequent use of vias interconnecting grounds on both sides of PCB or on different layers of the board may help lower RF impedance in the ground structure.

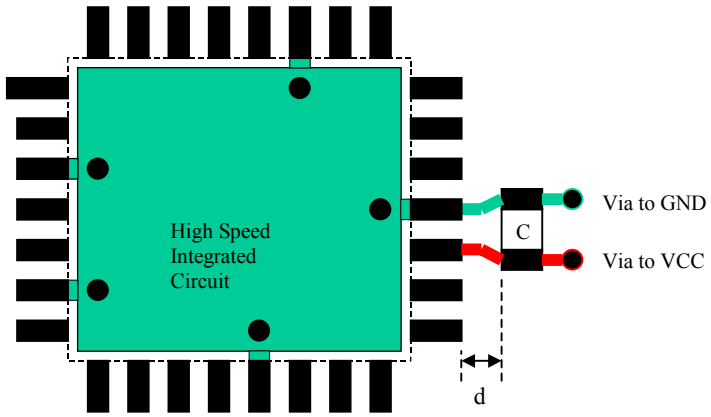


Figure 5–7. IC Ground

10. All ground planes, belonging to the same net, should be conductively tied together with low impedance connections at each component's ground pin.

11. Ground returns from high-frequency digital circuits and low-level analog circuits should never be mixed. Assure that ground return paths for analog, digital, or power signals don't flow through each other's circuits.

12. Keeping ground leads shorter than one-twentieth (1/20) of a wavelength may prevent excessive radiated emissions and may help to maintain low impedance.

13. Single-point grounding scheme should only be used for low level and low frequency circuits (below 1 MHz). Figure 3–3.

14. Multi-point grounding scheme should be used for high frequency circuits (above 1MHz) to keep ground impedance low. Figure 3–4.

15. Assure even distribution of ground pins across all connector pin fields (including ribbon cables or custom device packages) to prevent local ground upset due to transient currents. The number of connector ground pins required should be determined prior to start of layout (Figure 5–21).

16. There should be no floating metal of any kind near any PCB. All ground segments with length-to-width ratio greater than 10:1 should have, at the minimum, one GND via at each end tying them to rest of PCB ground structure. Figure 5–8.

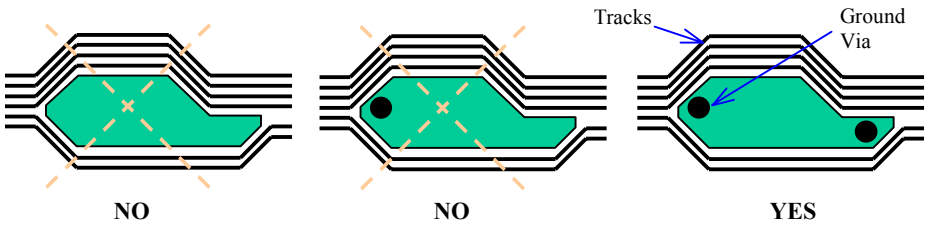


Figure 5–8. Eliminating Floating Ground

17. For PCBs without a ground plane, a minimum of one ground-return track should be routed adjacent to each eight lines of address and data lines to minimize the loop area. Keep the lines as short as possible. For the address lines, route the ground return next to the least significant bit (LSB) since this line is likely to be the most active.

18. Avoid ground loops. They can be the source of radiated emissions. A ground plane or ground grid are helpful in preventing ground loops from forming. Breaking a loop with small gap may work at DC but gap capacitance may effectively close the loop at higher frequencies, creating a large loop antenna. Apart from the RE problems, large ground loops are known to cause the system to be susceptible to malfunction when subjected to external EMI sources.

19. Extend ground planes as far as possible beyond the boundaries of components and their tracks and power planes – ground planes should extend beyond power planes and any tracks by at least 20 times their layer spacing (Figure 5–9).

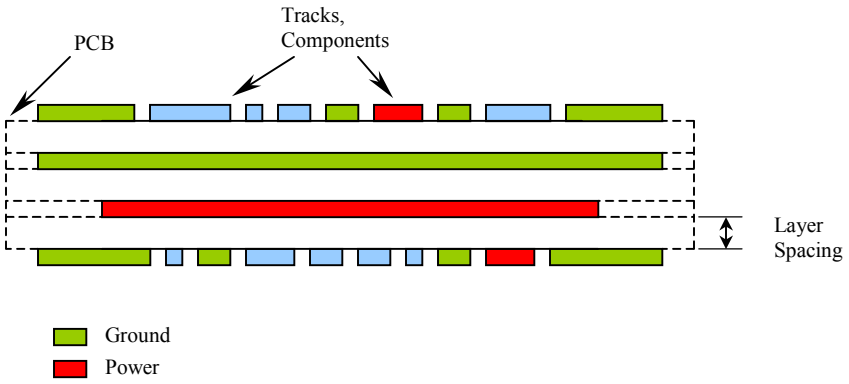


Figure 5–9. Establishing Ground Plane Boundary

5.2. Power Systems

20. Power supplies should be located close to power entry point to PCB, and as close as possible to powered circuitry. Closely routed tracks (to minimize the area between conductors, and hence the inductance) should be used to connect the power source to the local power distribution system.

21. Power feeds should always be decoupled at their entry points onto the PCB.

22. Bulk capacitors should always be parallel decoupled with one or more smaller high-frequency capacitors with low ESL (equivalent series inductance). Place the smallest value decoupling capacitor closest to a device to be decoupled.

23. Power should be distributed with a 'star', or grid, or power plane configuration but never with point-to-point wiring (daisy-chaining). Use the positive side of the bulk capacitor on the output of the voltage regulator as the "star" point (Figure 5–10).

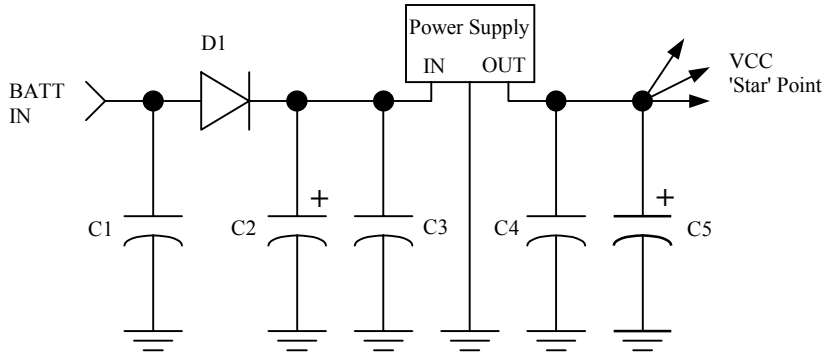


Figure 5–10. Power System's Star Point

24. The value of the bulk capacitor should be at least ten (10) times greater than the sum of all the values of decoupling capacitors.

25. High-frequency, low-inductance ceramic capacitors should be used for integrated circuit (IC) decoupling at each power pin – use 0.1 μF for up to 15 MHz, and 0.01 μF over 15 MHz. The decoupling capacitor should be located as close as physically possible from the IC's power pin. Figure 5–7.

    Power distribution system must provide sufficient current, in time, for the device to function properly. This includes high-peak current requirements during output switching. Local discrete capacitors, when placed next to the device and attached to power and ground with low inductance connections, will provide this current.

26. Printed circuit board traces which carry high switching current with fast rise/fall times (5 – 10 ns) should maintain at least 3 mm spacing from other signal traces which run parallel to them, and/or a ground guard traces should be placed between them.

27. Corresponding power and ground signals should always be routed in parallel (side-by-side) or on top of each other (on adjacent layers) to minimize loop area thus reducing loop impedance (Figure 5–11).

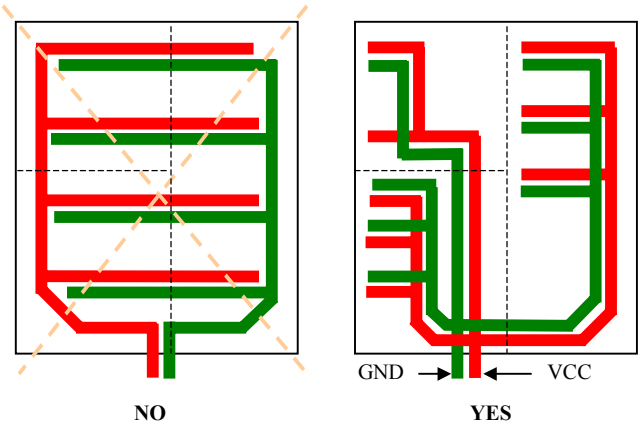


Figure 5–11. Power and Ground Routing

28. VCC (clean power) traces should never be routed parallel to unfiltered (dirty) traces that carry battery, ignition, high-current, or fast switching signals.

29. Use the lowest power, slowest logic that satisfies circuit requirements.

30. Power, ground, and signal traces on the board should be kept short and as wide as possible. The traces should be shorter than the diagonal dimension of the board, and ideally their length-to-width ratio should be kept at 10:1.

31. Placing ferrite beads on power tracks may provide attenuation of unwanted signals above 1 MHz. When properly sized, these beads can be very effective in damping high-frequency switching transients or parasitic ringing due to line reflections without causing a DC loss. CAUTION: using ferrites may impede AC current flow.

32. Devices sensing battery or ignition, such as sensing resistors, should be placed at the power entry point to PCB (close to I/O connector).

33. Devices, such as Zener diodes, MOV's or transzorbs should be placed at the power entry point to PCB as their function is to limit/clip transients and spikes. Assure low-impedance connection to ground.

34. Provide enough current storage (capacitor) on the incoming battery line when designing switching power supplies and/or other circuits drawing discontinuous currents from the battery, so that these currents do not appear on the wiring harness where they can be radiated or conducted to other circuits.

35. Closely grouped Power Switching and High Current circuits should be kept separate from digital, low level analog, and relay circuits.

36. All switching mode power supply (SMPS) traces should be routed on one layer of PCB with the SMPS reference plane placed directly on adjacent layer to minimize the loop area.

37. Heatsink of the power switching transistor should be connected to the same potential as the transistor's tab, either power or ground. Sometimes the heatsink is not directly connected to the power switching transistor, but is insulated from it by a dielectric material. This produces a parasitic capacitance between the power transistor and the heatsink. Attaching the heatsink to a reference plane other than the power or ground used by the power transistor may provide a path for common-mode currents.

38. The loop area of Switching Mode Power Supply (SMPS) snubber circuit should be as small as physically possible (Figure 5–12).

39. The primary loop area of SMPS that uses a transformer should be minimized as much as possible (Figure 5–12). The loop includes the positive lead of the bulk capacitor, the primary windings of the transformer, collector or drain of the switching transistor, current sense resistor; the ground lead of the current sense resistor, and the ground lead of the bulk capacitor.

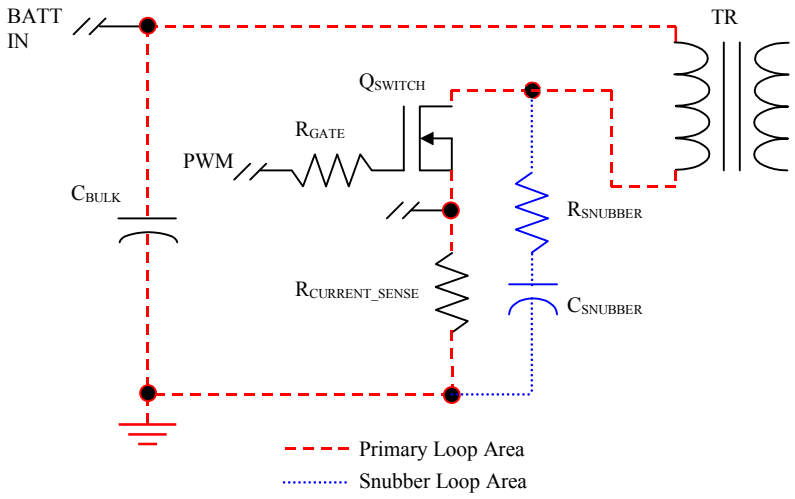


Figure 5–12. Primary Loop Area

40. The secondary loop area of SMPS that uses a transformer should be minimized as much as possible (Figure 5–13). The loop includes the positive side of the secondary windings of the transformer, the series diode, the bulk capacitor; the ground lead of the bulk capacitor, and the ground side of the secondary winding of the transformer.

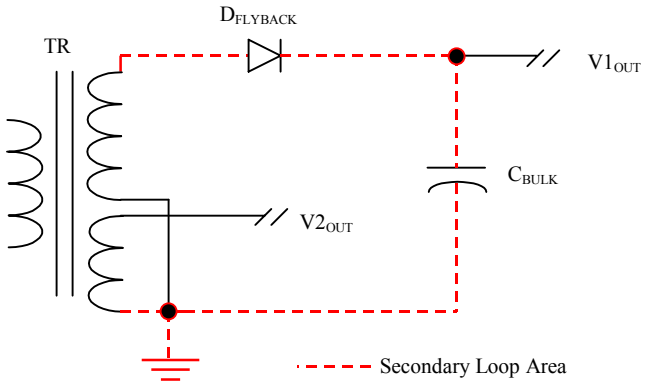


Figure 5–13. Secondary Loop Area

5.3. Digital Circuits

41. Digital clock connections (being very aggressive signals) should be the first 'nets' to be routed, and they should be run on a single PCB layer adjacent to a ground plane.

42. All clock/address/data bus connections should be as short and direct as possible with adjacent ground guard tracks or ground plane (Figure 5–14). Avoid using wires, stubs or ribbon cables to distribute clock signals.

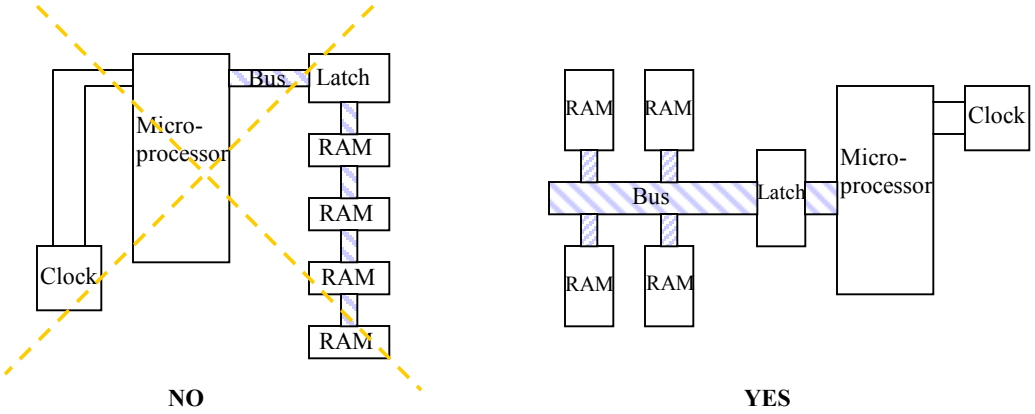
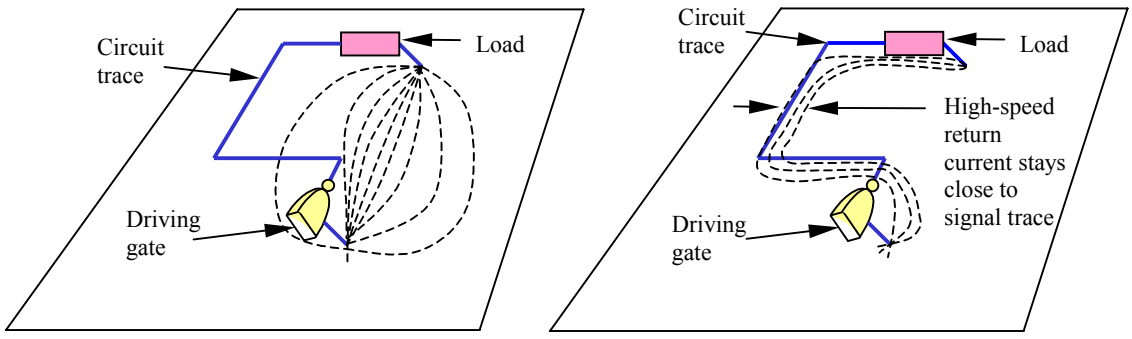


Figure 5–14. Minimizing Digital Bus Length

43. High-speed digital signals, such as data, address, and control lines of microprocessors, should be grouped together and located as far from the I/O connector as possible.

44. Always route signal tracks and their associated ground returns as close to one another as possible to minimize the area (loop) enclosed by current flow (Figure 5–15).



a) At low frequencies current follows the path of least resistance

b) At high-frequencies current follows the path of least inductance

Figure 5–15. Resistance and Inductance as Functions of Frequency

45. Avoid running any traces other than ground next to/under crystals or any other inherently noisy circuits.

46. Keep oscillators and clock generating IC's away from I/O connectors and close to the chips they service, to keep the loop area small.

47. Always choose the lowest clock frequency and slowest rise and fall time for digital signals that meets system requirements.

48. All critical nets, such as clocks, data strobes, etc., should be routed manually adjacent to ground tracks or ground plane.

49. Place crystals or resonators as close as physically possible to the device they service, and ideally on the same side of PCB. Minimize the track length between the oscillator and the IC (Figure 5–16).

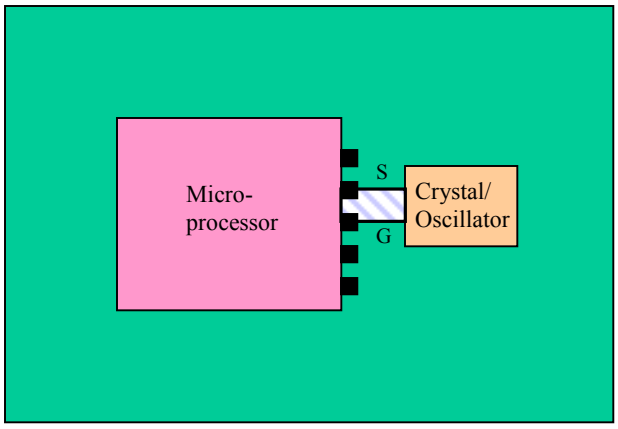


Figure 5–16. Crystal/Oscillator placement

50. Placing RF filters ahead of such components as diodes, transistors, or integrated circuits may prevent the RF from being converted to a DC or low frequency disturbance signals.

51. Using terminators for traces which length exceeds twice the signal rise time may prevent reflections at either end of a transmission line.

52. For long busses, keep high-speed traces separated from low speed signals by adding extra spacing between the high-speed and low-speed signals, and by running high frequency signals next to a ground trace.

53. All differential signal lines should be routed adjacent to one another to take full advantage of magnetic field cancellation. Place ground guard traces on both sides of the entire length of the differential-pair signals.

54. Routing signal tracks perpendicular (90˚) to each other on adjacent layers of a printed circuit board may help to minimize cross-talk.

55. Controlling the rise and fall times, the duty cycle, and the fundamental frequency of switched signals may help to minimize harmonic generation.

56. All unused IC inputs should be terminated to prevent unintentional random switching and noise generation – i.e. unterminated CMOS inputs tend to self-bias into a linear region of operation, significantly increasing the DC current drawn. Consult IC manufacturer for recommendations.

57. Provide good ground imaging for long traces, high speed signals.

58. Keep high-speed traces away from the edge of a PCB.

5.4. Analog Circuits

59. Analog or peripheral circuitry should be located as close to the I/O connector as possible, and be kept away from high speed digital, high current, or power switching circuits. Figure 5–2.

60. Routing of low level analog signals should be confined to analog section of PCB only.

61. Low pass filtering should always be used on all analog inputs.

62. Printed circuit board traces which terminate at the device connector should be decoupled of RF at the connector.

63. Ground guard tracks should always be routed adjacent to analog signals. Attach the guard tracks at both ends with vias to sending and receiving circuits' ground.

64. If using suppression device across coils of relays and/or solenoids the suppressor should be placed as close to the coil terminals as possible.

65. If a PWM signal is used to drive a solenoid, resistor suppression may be used. This will prevent high rate of change of current (di/dt), which can cause excessive magnetic field radiation.

66. Biasing resistors when placed as close as physically possible to the base of transistors may prevent RF from coupling in and turning the transistor on or off. (Figure 5–17)

67. Base and emitter bypass capacitors should be located very close to transistors (Figure 5–17). They should be connected to ground with low impedance connection to minimize inductance and loop area.

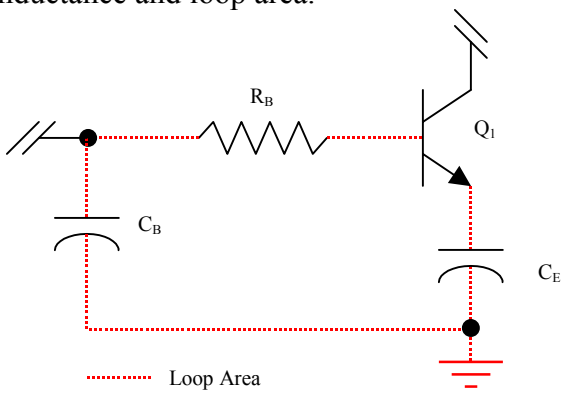


Figure 5–17. Transistor Circuit Routing

68. Treat every trace carrying sensitive signals (especially into high input impedance loads i.e. higher than 10 kΩ) as a receiving antenna when considering its routing.

5.5. Communication Protocols

69. SCP physical layer EMC layout guidelines should always be considered and followed. Use the latest revision available. For details refer to the following web site: http://www_eese.ford.com/mux

70. CAN physical layer EMC layout guidelines should always be considered and followed. Use the latest revision available. For details refer to the following web site: http://www_eese.ford.com/mux

71. UBP physical layer EMC layout guidelines should always be considered and followed. Use the latest revision available. For details refer to the following web site: http://www_eese.ford.com/mux

72. FORD ISO-9141 physical layer EMC layout guidelines should always be considered and followed. Use the latest revision available. For details refer to the following web site: http://www_eese.ford.com/mux

73. ACP physical layer EMC layout guidelines should always be considered and followed. Use the latest revision available. For details refer to the following web site: http://www_eese.ford.com/mux

74. Always consult Ford EMC representative prior to PCB layout when/if a communication protocol not listed here is considered for use in the design.

5.6. Shielding

75. All metallic shields of a system should be interconnected and grounded. Each shield ought to have a low-impedance contact to ground in at least two places in order to prevent its noise potential from coupling to the enclosed object. An ungrounded shield's potential will vary with conditions and location, and therefore the noise coupled to the object inside will vary also.

76. Placing a shield over the whole harness may limit radio frequency (RF) emissions from it. To reduce susceptibility and cross-talk between high impedance lines within a wiring harness use individual shields. Since shielding of harness is generally less cost-effective and more labor intensive than other EMI suppression measures such as filtering, it should not be the first choice in EMI suppression.

77. In order to realize shielding effectiveness, the shield ought to completely enclose the electronics eliminating any penetrations such as holes, seams, slots, or cables. Any penetrations in the shield unless properly treated, may drastically reduce the effectiveness of the shield.

78. Shields for low frequency signals (below 10 MHz) should be terminated and grounded only at the source, thus preventing undesirable ground loops (Figure 5–18).

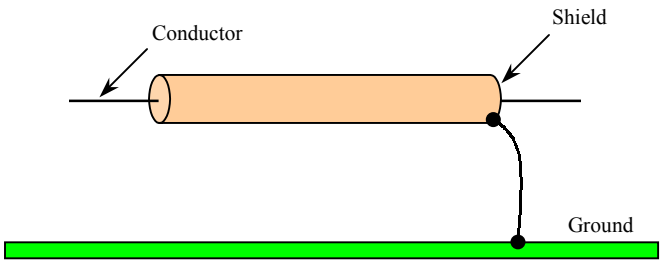


Figure 5–18. Shielding of Low-Frequency Signals

79. Shields for frequency signals (above 10 MHz) should be terminated and grounded at both ends (Figure 5–19).

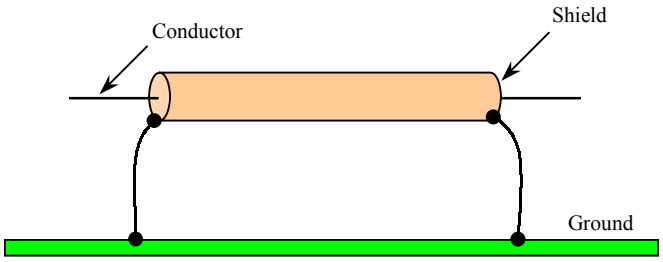


Figure 5–19. Shielding of High-Frequency Signals

80. Using twisted-pair wiring to the load should avoid creation of loop antennas that can radiate magnetic fields.

81. When routing a wire harness along sheet metal keep it away from any openings as much as possible. Openings may act as slot antennas.

82. Keep wire harness at least 5 inches away from electric field sources such as distributors and magnetic field sources such as alternators and solenoids.

83. The exposed (unshielded) end of a shielded cable near a connector or a terminal should not exceed 10 mm in length.

84. Always try to minimize the length of wire harness to reduce coupling and pickup.

85. Use twisted pair for sensitive low-frequency signals (below 1.0 MHz) and for circuits with impedances less than 1.0 kΩ to provide accurate reference voltages.

86. Coaxial cable should be used for transmission of RF (above 10 MHz) and where impedance match over a broad frequency range is important (such as video applications).

87. Circuits generating large, abrupt current variations should be provided with a separate return lead to the ground in order to reduce transient pickup in other circuits.

5.7. Miscellaneous

88. All unused multipurpose Integrated Circuit (IC) ports should be configured as outputs to prevent unintentional random state switching and noise generation – i.e. unterminated CMOS inputs tend to self-bias into the linear region of operation, thus significantly increasing DC current draw. Use appropriate pull-up or pull-down discrete components. Consult IC manufacturer for recommendation.

89. Software may be used to disable (turn off) all unused clock outputs from an IC. Consult IC manufacturer for recommendation.

90. Reducing output buffer drive from IC's may reduce radiated emissions. Consult IC manufacturer for recommendations.

91. All output drivers should be protected against flyback transient from inductive loads.

92. ESD sensitive devices should never be located close to I/O connectors or any other accessible openings where they may be damaged by an ESD event.

93. Keep ribbon cables and jumper strips away from IC's and oscillator circuits. Routing over or near IC's should be avoided at all cost (Figure 5–20).

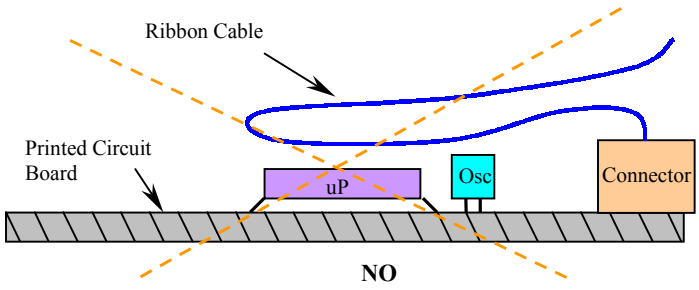


Figure 5–20. Packaging Considerations Affecting RE and CE

94. When attaching ribbon cables to PCB's always provide multiple ground returns to minimize loop area (Figure 5–21).

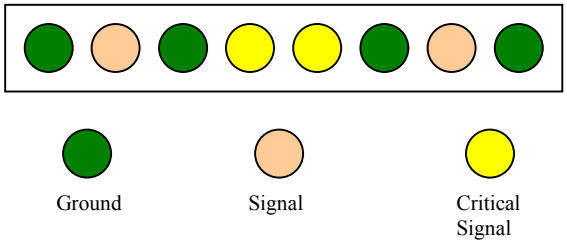


Figure 5–21. Use of Interspersed Grounds

95. Critical signals should never be placed on the outside conductors of shielded ribbon cables (Figure 5–21).

.

PART VI: REQUIREMENTS

6. MANAGEMENT OF CHANGE FOR EMC

Electronic modules are often changed after their initial release for many reasons and each change must be evaluated for its potential impact on the EMC performance. It is a regular dilemma as to which EMC tests to repeat if at all. Repeating all tests is the safest answer but not cost effective. So it is necessary to define a logical process for considering the performance of original module and the potential impact of the change.

Evaluating the exact impact of a change on the final EMC performance is not very easy and requires in depth understanding of both electronic and electromagnetic characteristic of the module. The product designers and the EMC experts of the module's supplier are best placed to analyze the change and decide which EMC tests to repeat. Here at Ford, we expect to be advised by the supplier as to what is changed, the analysis of the expected impact on EMC characteristics and what tests shall be repeated. We will review suppliers' analysis and may request additional tests as we see fit based on the information provided.

It is proposed that the following process is used for establishing what tests are to be run:
(Only tests that were deemed to be applicable in the initial tests should be considered)

Repeat RE310 tests if one or all of the following statements are true:

- The change involved a software modification[1]
- The change resulted in a modified printed circuit board[2]
- Changes in any clock or PWM frequency, duty rate or other relevant parameter
- If the module is in a metallic housing and it has been modified in some way
- Any other change that can reasonably be expected to influence radiated emissions profile

6.1. Radiated Immunity:

6.1.1. For safety critical systems (containing one or more Class C functions)

Repeat RI 11X tests if change influences items listed for RE310 or any other change that can reasonably be expected to influence radiated immunity profile.

Repeat RI120 and RI130 if the change impacts any aspect of input / output interface (changes to hardware or software)

Repeat RI140 if the change involves any items that are sensitive to magnetic fields

6.1.2 For non-safety critical systems

Repeat RI120 and RI130 if the change impacts any aspect of input / output interface (changes to hardware or software)

Repeat RI140 if the change involves any items that are sensitive to magnetic fields

If the change involved any of the modifications listed for radiated missions listed above, run radiated emissions first. If the results are different (+/- 3 dB in amplitude and +/- 1 MHz in frequency) compared to the original data then repeat the RI11x series of Radiated Immunity tests.

6.2. Conducted immunity:

Repeat CI210, CI220, CI230, CI240, CI260 and CI270 tests if the change influences any of the circuit interfaces directly or indirectly connected to the vehicle supply network.

- Changes to the component specification such as package size, value or rating
- The placement or routing changes influencing component specifically intended for EMC mitigation
- Change involved a voltage regulator or any associated circuitry such as capacitors, resistors, indictors or active components such as diodes, transistors or supply voltage watchdogs.

In addition consider repeating CI260 if there has been software change that results in a different operating loop time or influences power supply or reset management.

6.3. Electrostatic Discharge

Repeat CI280 A if the change involved any modification to parts or PCB associated or within close proximity (within 25mm) of external connector pins.

Repeat CI280B and/or CI280C tests if there has been a change to module packaging such as changing case material type, addition of metallic labels, and changing aperture sizes.

It is also necessary to consider the impact of PCB changes if the PCB is part of the man machine interface such as boards that contain displays or push buttons.

[1] Any modifications to module's software which influence the core operating routine, power supply management, communications, input output management or similar parts which can reasonable be expected to result in different radiated emissions profile.

[2] Any modifications to printed circuit board (PCB), which result in a change of the substrate material or on the copper area resulting from actions such as moving components, rerouting tracks, redefining earth fills, movement, deletion or addition of vias (layer to layer interconnections).

6.4. Conducted Emissions:

6.4.1 CE420 Frequency domain

Repeat if RE310 is run and the results are different ((+/- 3 dB in amplitude and +/- 1 MHz in frequency) in the band of 0.15 – 108 MHz,

or

If the change involves any parts that are used for controlling conducted emissions such as suppression components,

or

Any other change that can reasonably be expected to influence conducted emissions profile.

6.4.2 CE410 Time Domain

Repeat if conditions for Conducted Immunity listed above are met.

Table 6–1. Analysis of EMC Testing

	Test	Reasons for NOT testing
Radiated Immunity	RI 110	
	RI 120	
	RI 130	
	RI 140	
Conducted Immunity	CI 210	
	CI 220	
	CI 230	
	CI 240	
	CI 250	
	CI 260	
	CI 270	
	CI 280 (A)	
	CI 280 (B)	
	CI 280 (C)	
Radiated Emissions	RE 310	
Conducted Emissions	CE 410	
	CE 420	

Note: Use this table to record your own analysis

PART VII: CHECKOFF LIST

7. CHECKOFF LIST – EMC DESIGN GUIDE FOR PCB(S)

The following list shall be completed and submitted to the approving activity, together with the EMC test plan, at least 60 days prior to commencement of component level EMC testing.

7.1. *General description*

ESC Name: _____

Manufacturer: _____

Ford P/N(s): _____ PWB #: _____

Model Year: _____ Vehicle Application: _____

7.2. *Physical segregation of circuits has been employed right from the beginning of PCB design*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.3. *All relevant components/tracks have been contained within their designated PCB area*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.4. *Which type of Power distribution technique best describes the PCB?*

- ☐ N/A
- ☐ Minimal (daisy chain) distribution
- ☐ Single-point (star) distribution
- ☐ Power plane
- ☐ Other, explain: _____

7.5. *Which type of Ground distribution technique best describes the PCB?*

- ☐ Minimal (daisy chain)
- ☐ Single-Point (star)
- ☐ Multi-point
- ☐ Hybrid
- ☐ Ground grid
- ☐ Ground plane
- ☐ Other, explain: _____

7.6. *List <u>all</u> Power (voltage) levels present on PCB, and specify which ground they reference*

Power Level (Volts)	Reference Ground
(Example: 3.3 VDC)	*(Example: Logic ground)*

7.7. *List PCB layer stack-up and content, indicating the location of all crystal(s)/resonator(s)*

Layer number	Layer content
Layer 1	
Layer 2	
Layer 3	
Layer 4	
Layer 5	
Layer 6	

7.8. *All possible surface areas of the PCB have been filled with ground*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.9. *All ground segments have been tied together with multiple vias and/or with many short thick tracks, and there is no 'floating' copper of any kind on the PCB*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.10. *List names and provide actual track lengths as well as rise/fall time of all periodic clock signals (e.g. ECLK, MCLK, ALE, CLKOUT, etc.)*

Signal name	Signal length (mm)	Signal rise time (t_r)	Signal fall time (t_f)

7.11. *All clock signals have adjacent ground-return tracks*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.12. *All unused connector pins have been terminated to PCB ground*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.13. *The PCB contains the following communications protocols:*

- ☐ N/A
- ☐ ACP
- ☐ CAN
- ☐ ISO-9141
- ☐ SCP
- ☐ UBP
- ☐ Other, explain: _____

7.14. *Discrete components supporting the individual communication protocols, also known as physical layers, have been placed and routed according to their unique EMC design requirements as specified by Ford -- list the applicable specification used**

- ☐ N/A
- ☐ ACP . . . . . Spec.#: _____
- ☐ CAN . . . . . Spec.#: _____
- ☐ ISO-9141 . . . Spec.#: _____
- ☐ SCP . . . . . Spec.#: _____
- ☐ UBP . . . . . Spec.#: _____
- ☐ Other, explain: _____

7.15. *Potential radiated emissions from CPU(s) have been considered prior to PCB layout*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.16. *List and classify each CPU according to its highest radiated emissions level***

CPU Name	IC RE Reference Level

7.17. *Has the PCB been grounded to its enclosure (housing)? Specify type of connection*

- ☐ N/A (non-metallic housing)
- ☐ Yes => ☐ DC connection ☐ AC connection
- ☐ No
- ☐ If No, explain: _____

7.18. *Unused clock outputs from CPU(s) have been addressed to minimize radiated emissions (i.e. proper termination, disabled in software)*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.19. *EMC support has been available throughout the PCB layout phase*

- ☐ N/A
- ☐ Yes
- ☐ No
- ☐ If No, explain: _____

7.20. *Please provide the name, company, job title, and contact information of the person(s) responsible for EMC signoff of this product*

Name:	
Company:	
Job Title:	
Phone #:	
E-mail:	

Note:

* Recommended EMC design guidelines for each physical layer are available form Ford's external web site at – http://www_eese.ford.com/mux.

** For IC RE reference levels refer to Ford's General IC Specification Limits for Radiated Emissions, part number ES-3U5T-1B257-AA, 10/01/2002 or latest revision.

Collected References:

XW7T-1A278-AB, *Component Specification Electromagnetic Compatibility*, Ford Motor Company, April 1999

C.R. Paul, *Introduction to Electromagnetic Compatibility*, John Wiley Interscience, 1992

A.R. Macko, *Electromagnetic Compatibility and Electromagnetic Interference Control in the Automotive Electrical Environment*, Ford/Visteon/EMCARM Co., 1995

A.R. Macko, A. Nielsen, P. Bator, *Electromagnetic Compatibility for Printed Circuits Boards*, Ford Motor Company/Visteon, December, 1994

A. Gunsaya, *Management of Change for EMC*, Ford Motor Company, March 2002

H.W. Ott, *Noise Reduction Techniques in Electronic Systems*, Second Edition, John Wiley Interscience, 1998

Howard W. Johnson, Martin Graham, *High-Speed Digital Design*, Prentice Hall, 1993

Michel Mardiguian, *Interference Control in Computers and Microprocessor-Based Equipment*, First Edition, Don White Consultants, 1987

Mike Catherwood, *Designing for Electromagnetic Compatibility (EMC) with CMOS Microcontrollers*, Document Ref. No. AN1050, Motorola, Inc.

Imad Kobeissi, *Noise Reduction Techniques for Microcontroller-Based Systems*, Document Ref. No. AN1705, Motorola, Inc.

Hewlett-Packard, *Designing for Electromagnetic Compatibility*, Student Workbook, Course No. HP 11949A, Hewlett-Packard Company, 1989

Darryl Lindsey, *The Design & Drafting of Printed Circuits*, Revised Edition, Bishop Graphics, Inc. 1984

Keith Armstrong, *PCB Design Techniques for Lowest-Cost EMC Compliance*, Part 1, Electronics and Communication Engineering Journal, August 1999

Jean-Claude Kedzia, Giuseppe Guglielmetti, Stefan Dickmann, *Improving EMC Compliance of Electronic Devices through Numerical Simulation*, EC project, BRPR-CT97-0592